Si823x

0.5 AND 4.0 AMP ISODRIVERS (2.5 AND 5 kV_{RMS})

Features

- Two completely isolated drivers in one package
  - Up to 5 kV_{RMS} input-to-output isolation
  - Up to 1500 V_{DC} peak driver-to-driver differential voltage
- HS/LS and dual driver versions
- Up to 8 MHz switching frequency
- 0.5 A peak output (Si8230/1/2)
- 4.0 A peak output (Si8233/4/5/6)
- 60 ns maximum propagation delay
- Independent HS and LS inputs or PWM input versions
- Transient immunity >30 kV/µs
- Overlap protection and programmable dead time
- Operating temperature range –40 to +125 °C
- UL/VDE/CSA approval
- RoHS-compliant

Applications

- Power delivery systems
- Motor control systems
- Isolated dc-dc power supplies
- Lighting control systems
- Plasma displays
- Solar and industrial inverters

Description

The Si823x isolated driver family combines two independent, isolated drivers into a single package. The Si8230/1/3/4 are high-side/low-side drivers, and the Si8232/5/6 are dual drivers. Versions with peak output currents of 0.5 A (Si8230/1/2) and 4.0 A (Si8233/4/5/6) are available. All drivers operate with a maximum supply voltage of 24 V.

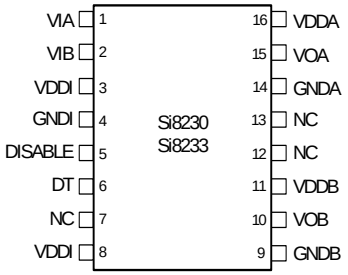
The Si823x drivers utilize Silicon Labs' proprietary silicon isolation technology, which provides up to 5 kV_{RMS} withstand voltage per UL1577, and fast 60 ns propagation times. Driver outputs can be grounded to the same or separate grounds or connected to a positive or negative voltage. The TTL level compatible inputs with >400 mV hysteresis are available in individual control input (Si8230/2/3/5/6) or PWM input (Si8231/4) configurations. High integration, low propagation delay, small installed size, flexibility, and cost-effectiveness make the Si823x family ideal for a wide range of isolated MOSFET/IGBT gate drive applications.

Safety Approval

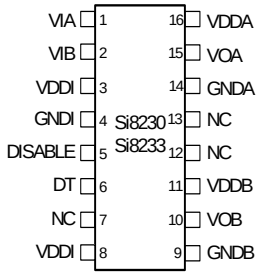
- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA component notice 5A approval
  - IEC 60950, 61010, 60601 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-2 (VDE 0884 Part 2)
  - EN 60950 (reinforced insulation) (Pending)

Pin Assignments

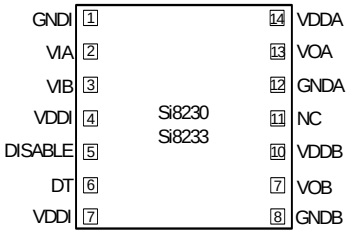
SOIC-16 (Wide)



SOIC-16 (Narrow)



LGA-14 (5 x 5 mm)



Patents Pending

Block Diagrams

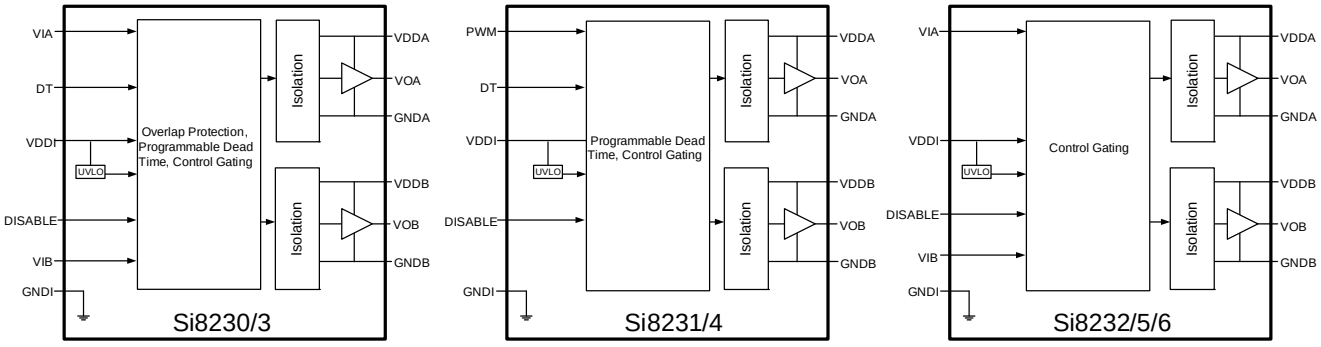


TABLE OF CONTENTS

Section **Page**

1. Top-Level Block Diagrams

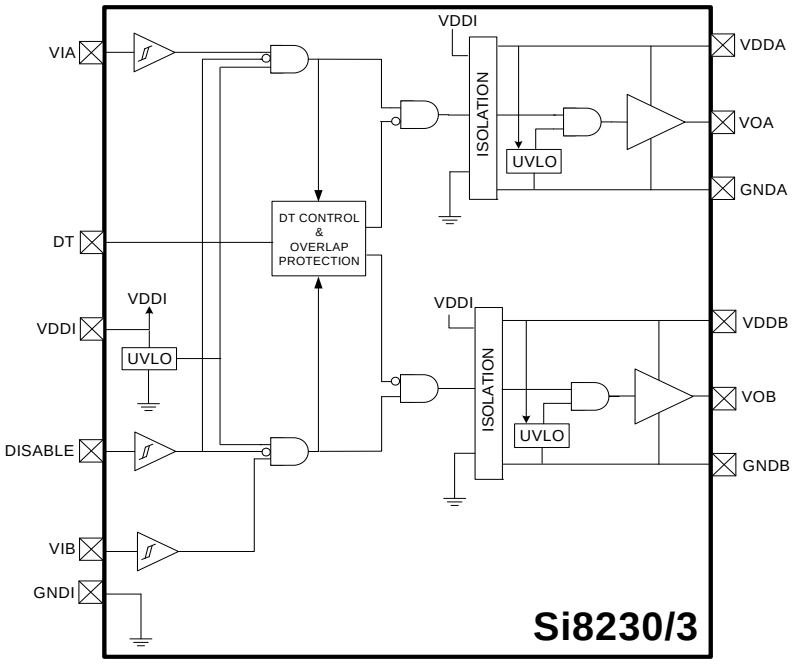


Figure 1. Si8230/3 Two-Input High-Side / Low-Side Isolated Drivers

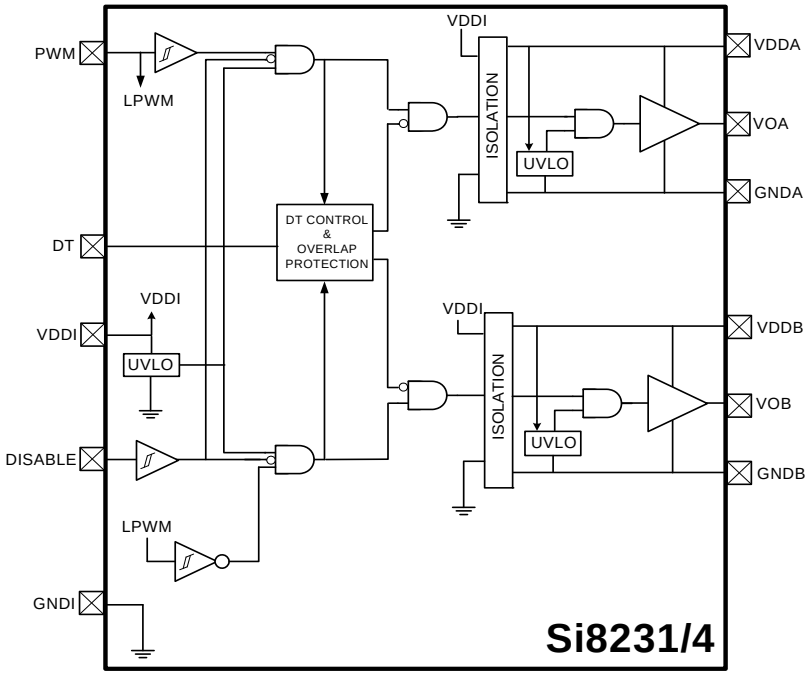


Figure 2. Si8231/4 Single-Input High-Side / Low-Side Isolated Drivers

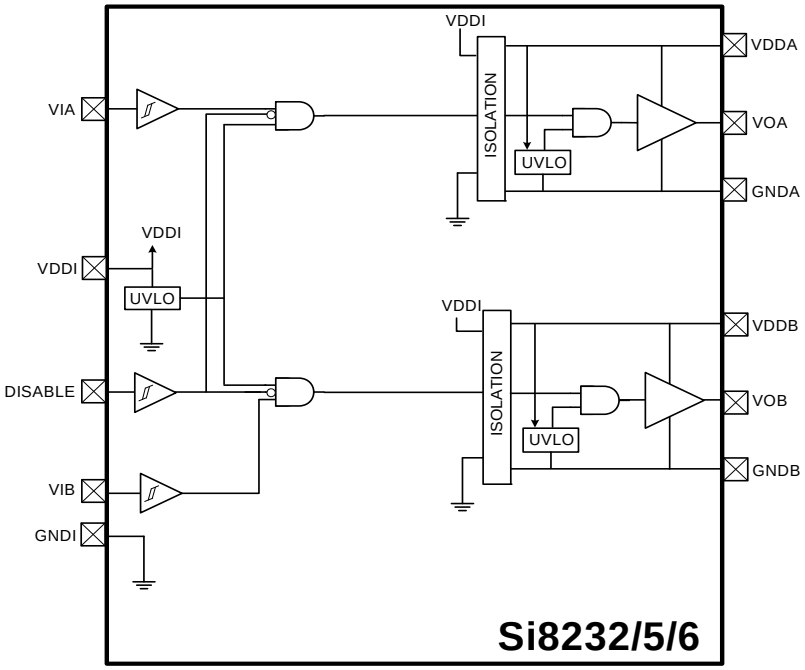


Figure 3. Si8232/5/6 Dual Isolated Drivers

2. Electrical Specifications

Table 1. Electrical Characteristics[1]

4.5 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DC Specifications						
Input-side Power Supply Voltage	VDDI		4.5	—	5.5	V
Driver Supply Voltage	VDDA, VDDB	Voltage between VDDA and GNDA, and VDDB and GNDB (See “9. Ordering Guide”)	6.5	—	24	V
Input Supply Quiescent Current	IDDI(Q)	Si8230/32/33/35/36	—	2	3	mA
		Si8231/34	—	2	3	mA
Output Supply Quiescent Current	IDDA(Q), IDDB(Q)	Current per channel	—	—	3.0	mA
Input Supply Active Current	IDDI	PWM freq = 500 kHz	—	2.5	—	mA
Output Supply Active Current	IDDO	PWM freq = 500 kHz	—	3.6	—	mA
Input Pin Leakage Current	IVIA, IVIB, IPWM		–10	—	+10	µA dc
Input Pin Leakage Current	IDISABLE		–10	—	+10	µA dc
Logic High Input Threshold	VIH		2.0	—	—	V
Logic Low Input Threshold	VIL		—	—	0.8	V
Input Hysteresis	VI_{HYST}		400	450	—	mV
Logic High Output Voltage	VOAH, VOBH	IOA, IOB = –1 mA	(VDDA /VDDB) — 0.04	—	—	V
Logic Low Output Voltage	VOAL, VOBL	IOA, IOB = 1 mA	—	—	0.04	V
Output Short-circuit Pulsed Sink Current	IOA(SCL), IOB(SCL)	Si8230/1/2, Figure 4	—	0.5	—	A
		Si8233/4/5/6, Figure 4	—	4.0	—	
Output Short-circuit Pulsed Source Current	IOA(SCH), IOB(SCH)	Si8230/1/2, Figure 5	—	0.25	—	
		Si8233/4/5/6, Figure 5	—	2.0	—	
Output Sink Resistance	$R_{ON(SINK)}$	Si8230/1/2	—	5.0	—	Ω
		Si8233/4/5/6	—	1.0	—	
Output Source Resistance	$R_{ON(SOURCE)}$	Si8230/1/2	—	15	—	
		Si8233/4/5/6	—	2.7	—	

Notes:
1. VDDA = VDDB = 12 V for 5, 8, and 10 V UVLO devices; VDDA = VDDB = 15 V for 12.5 V UVLO devices.
2. TDD is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).
3. The largest RDT resistor that can be used is 220 kΩ.

Table 1. Electrical Characteristics[1] (Continued)

4.5 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising	3.60	4.0	4.45	V
VDDI Undervoltage Threshold	$VDDI_{UV-}$	VDDI falling	3.30	3.70	4.15	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$		—	250	—	mV
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV+}$, $VDDB_{UV+}$	VDDA, VDDB rising				
5 V threshold		See Figure 36 on page 25.	5.20	5.80	6.30	V
8 V threshold		See Figure 37 on page 25.	7.50	8.60	9.40	V
10 V threshold		See Figure 38 on page 25.	9.60	11.1	12.2	V
12.5 V threshold		See Figure 39 on page 25.	12.4	13.8	14.8	V
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV-}$, $VDDB_{UV-}$	VDDA, VDDB falling				
5 V threshold		See Figure 36 on page 25.	4.90	5.52	6.0	V
8 V threshold		See Figure 37 on page 25.	7.20	8.10	8.70	V
10 V threshold		See Figure 38 on page 25.	9.40	10.1	10.9	V
12.5 V threshold		See Figure 39 on page 25.	11.6	12.8	13.8	V
VDDA, VDDB Lockout hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 5 V	—	280	—	mV
VDDA, VDDB Lockout hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 8 V	—	600	—	mV
VDDA, VDDB Lockout hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 10 V or 12.5 V	—	1000	—	mV
AC Specifications						
Minimum Pulse Width			—	10	—	ns
Propagation Delay	t_{PHL}, t_{PLH}	CL = 200 pF	—	30	60	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD		—	—	5.60	ns
Minimum Overlap Time[2]	TDD	DT = VDDI, No-Connect	—	0.4	—	ns
Programmed Dead Time[3]	DT	Figure 41, RDT = 100 k	—	900	—	ns
		Figure 41, RDT = 6 k	—	70	—	ns
Output Rise and Fall Time	t_R,t_F	C_L = 200 pF (Si8230/1/2)	—	—	12	ns
		C_L = 200 pF (Si8233/4/5/6)	—	—	20	ns

Notes:

1. VDDA = VDDB = 12 V for 5, 8, and 10 V UVLO devices; VDDA = VDDB = 15 V for 12.5 V UVLO devices.
2. TDD is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).
3. The largest RDT resistor that can be used is 220 kΩ.

Table 1. Electrical Characteristics[1] (Continued)

4.5 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V. TA = –40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Shutdown Time from Disable True	t_{SD}		—	—	60	ns
Restart Time from Disable False	$t_{RESTART}$		—	—	60	ns
Device Start-up Time	t_{START}	Time from VDD_ = VDD_UV+ to VOA, VOB = VIA, VIB	—	5	7	µs
Common Mode Transient Immunity	CMTI	VIA, VIB, PWM = VDDI or 0 V	30	50	—	kV/µs

Notes:

1. VDDA = VDDB = 12 V for 5, 8, and 10 V UVLO devices; VDDA = VDDB = 15 V for 12.5 V UVLO devices.
2. TDD is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).
3. The largest RDT resistor that can be used is 220 kΩ.

2.1. Test Circuits

Figures 4 and 5 depict sink current and source current test circuits.

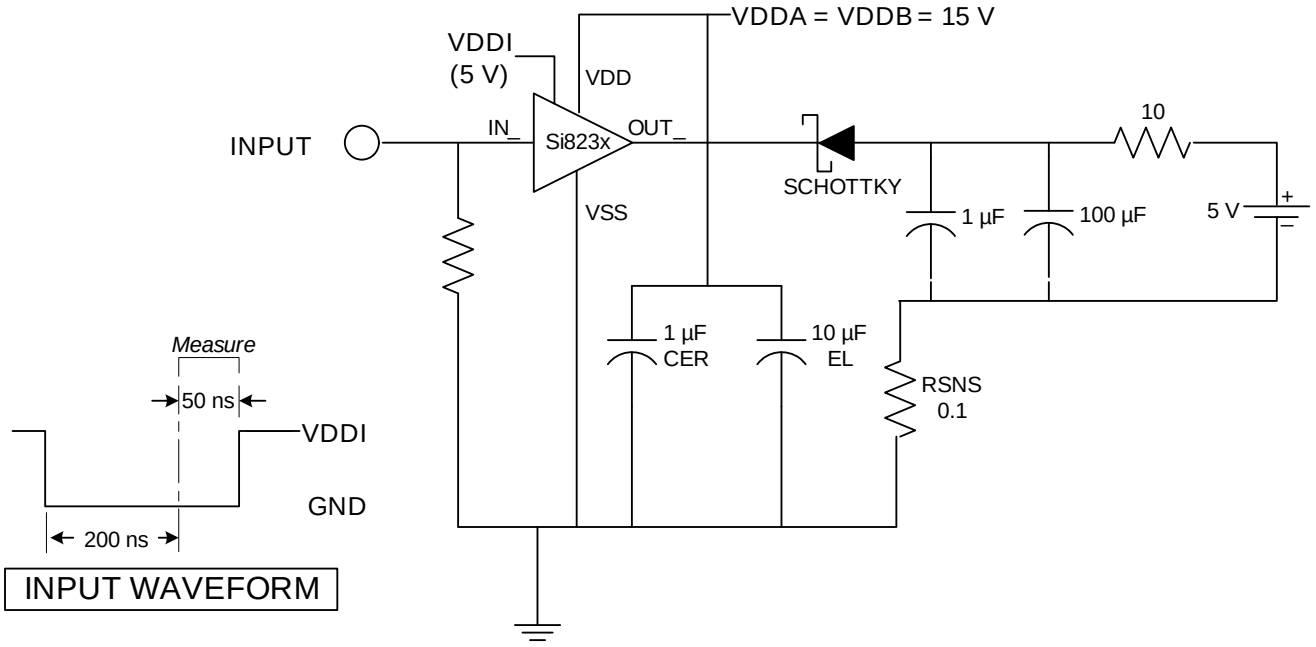


Figure 4. Sink Current Test Circuit

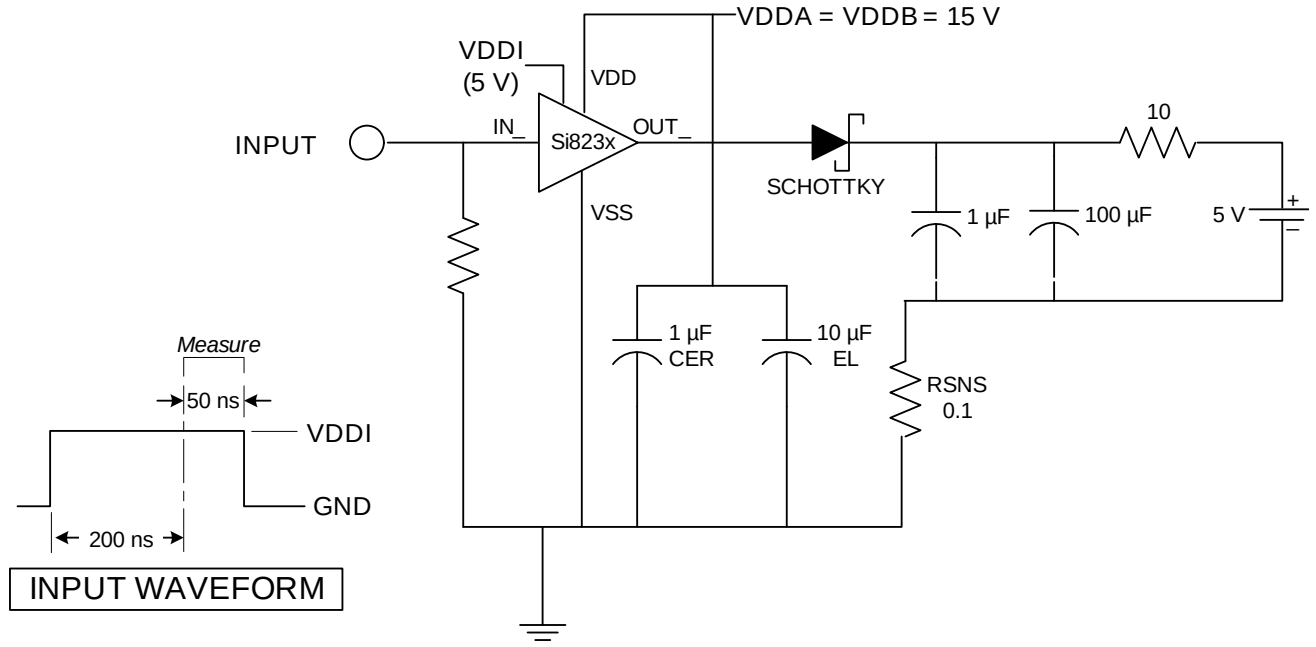


Figure 5. Source Current Test Circuit

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Units
Storage Temperature[2]	T_{STG}	–65	—	+150	°C
Ambient Temperature under Bias	T_A	–40	—	+125	°C
Input-side Supply Voltage	VDDI	–0.6	—	6.0	V
Driver-side Supply Voltage	VDDA, VDDB	–0.6	—	30	V
Voltage on any pin with respect to ground	VIN	–0.5	—	VDD + 0.5	V
Output Drive Current per channel	I_O	—	—	10	mA
Lead Solder Temperature (10 sec.)		—	—	260	°C
Maximum Isolation (Input to Output) (1 sec) WB SOIC-16		—	—	6500	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) WB SOIC-16		—	—	2500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) NB SOIC-16		—	—	4250	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) NB SOIC-16		—	—	2500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) 14 LD LGA without thermal pad		—	—	3850	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) 14 LD LGA without thermal pad		—	—	650	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) 14 LD LGA with thermal pad		—	—	1850	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) 14 LD LGA with thermal pad		—	—	0	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VDE certifies storage temperature from –40 to 150 °C.

Table 3. Regulatory Information*

CSA
The Si823x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
VDE
The Si823x is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
UL
The Si823x is certified under UL1577 component recognition program. For more details, see File E257455.
***Note:** Regulatory Certifications apply to 1.5 kV_{RMS} rated devices which are production tested to 1.8 kV_{RMS} for 1 sec. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec. For more information, see "9.Ordering Guide" on page 37.

Table 4. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value				Unit
			WBSOIC-16 5 kV_{RMS}	NBSOIC-16 WBSOIC-16 2.5 kV_{RMS}	14 LD LGA 2.5 kV_{RMS}	14 LD LGA w/ Pad 1.5 kV_{RMS}	
Nominal Air Gap (Clearance)[1]	L(1O1)		8.0	4.01	3.5	1.75	mm
Nominal External Tracking (Creepage)[1]	L(1O2)		8.0	4.01	3.5	1.75	mm
Minimum Internal Gap (Internal Clearance)			0.014	0.014	0.014	0.014	mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN IEC 60112/VDE 0303 Part 1	>175	>175	>175	>175	V
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1.4	1.4	1.4	1.4	pF
Input Capacitance[3]	C_I		4.0	4.0	4.0	4.0	pF

Notes:

1. The values in this table correspond to the nominal creepage and clearance values as detailed in “10. Package Outline: 16-Pin Wide Body SOIC” , “12. Package Outline: Narrow Body SOIC” , “14. Package Outline: 14 LD LGA (5 x 5 mm)” , and “16. Package Outline: 14 LD LGA with Thermal Pad (5 x 5 mm)” . VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC 16 and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si823x is converted into a 2-terminal device. Pins 1–8 (1-7, 14 LD LGA) are shorted together to form the first terminal and pins 9–16 (8-14, 14 LD LGA) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 5. IEC 60664-1 (VDE 0884 Part 2) Ratings

Parameter	Test Conditions	Specification			
		WB SOIC-16	NB SOIC-16	14 LD LGA	14 LD LGA w/ Pad
Basic Isolation Group	Material Group	IIIa	IIIa	IIIa	IIIa
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV	I-III	I-III	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-III	I-II	I-II	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-III	I-II	I-II	I-I

Table 6. IEC 60747-5-2 Insulation Characteristics*

Parameter	Symbol	Test Condition	Characteristic			Unit
			WB SOIC-16	NB SOIC-16 14 LD LGA	14 LD LGA w/ Pad	
Maximum Working Insulation Voltage	V_{IORM}		891	560	373	V peak
Input to Output Test Voltage	V_{PR}	Method a After Environmental Tests Subgroup 1 (V_{IORM} x 1.6 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	1590	896	597	V peak
		Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1375	1050	700	
		After Input and/or Safety Test Subgroup 2/3 (V_{IORM} x 1.2 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	1018	672	448	
Highest Allowable Overvoltage (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}		6000	4000	2650	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	$>10^9$	Ω

***Note:** The Si823x is suitable for basic electrical isolation within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si823x provides a climate classification of 40/125/21.

Table 7. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	WB SOIC-16	NB SOIC-16	14 LD LGA	14 LD LGA w/ Pad	Unit
Case Temperature	T_S		150	150	150	150	°C
Safety Input Current	I_S	θ_{JA} = 100 °C/W (WB SOIC-16), 105 °C/W (NB SOIC-16, 14 LD LGA), 50 °C/W (14 LD LGA w/ Pad) V_{DDI} = 5.5 V, V_{DDA} = V_{DDB}= 24 V, T_J = 150 °C, T_A = 25 °C	50	50	50	100	mA
Device Power Dissipation[2]	P_D		1.2	1.2	1.2	1.2	W

Notes:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figure 6.
2. The Si823x is tested with V_{DDI} = 5.5 V, V_{DDA} = V_{DDB} = 24 V, T_J = 150 ºC, C_L = 100 pF, input 2 MHz 50% duty cycle square wave.

Table 8. Thermal Characteristics

Parameter	Symbol	WB SOIC-16	NB SOIC-16	14 LD LGA	14 LD LGA w/ Pad	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	100	105	105	50	°C/W

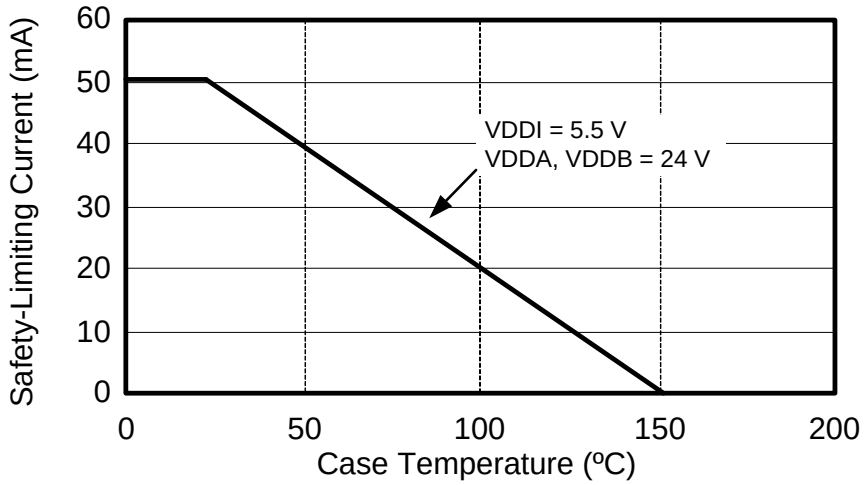


Figure 6. WB SOIC-16, NB SOIC-16, 14 LD LGA Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

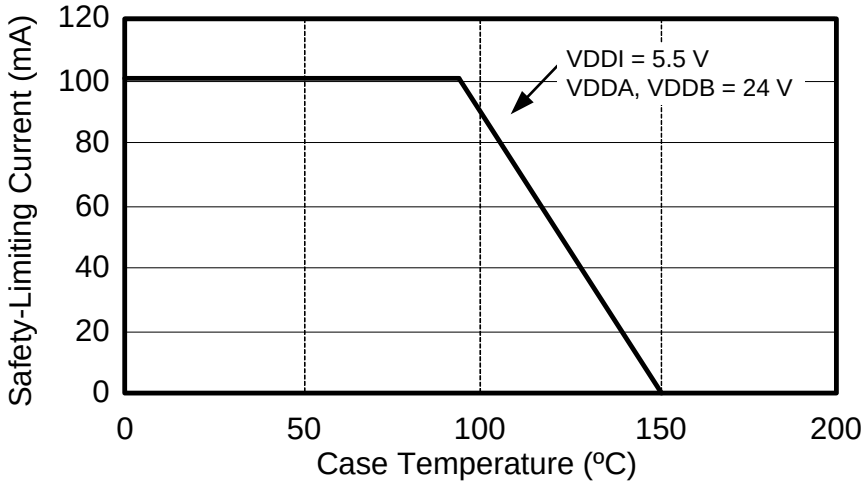


Figure 7. 14 LD LGA with Pad Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

2.2. Theory of Operation

The operation of an Si823x channel is analogous to that of an opto coupler and gate driver, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si823x channel is shown in Figure 8.

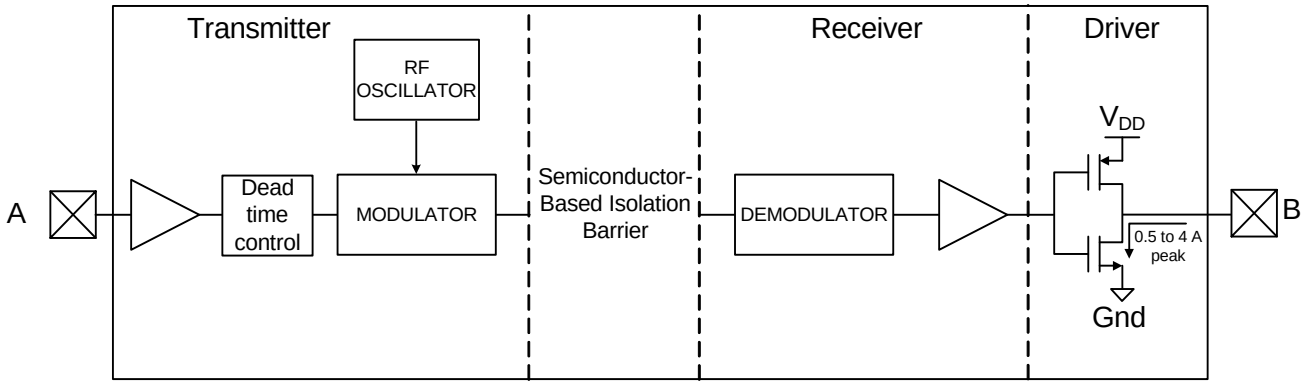


Figure 8. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 9 for more details.

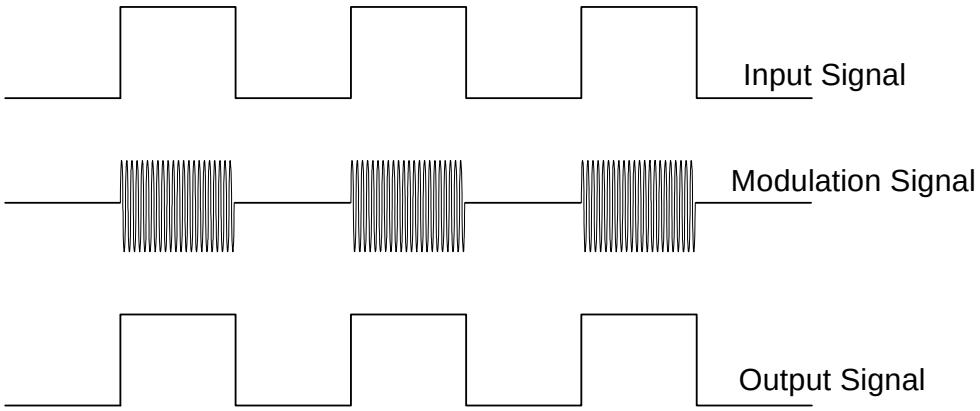


Figure 9. Modulation Scheme

3. Typical Operating Characteristics (0.5 Amp)

The typical performance characteristics depicted in Figures 10 through 21 are for information purposes only. Refer to Table 1 on page 6 for actual specification limits.

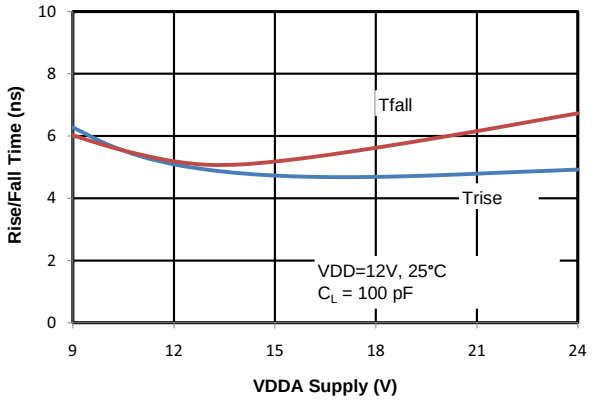


Figure 10. Rise/Fall Time vs. Supply Voltage

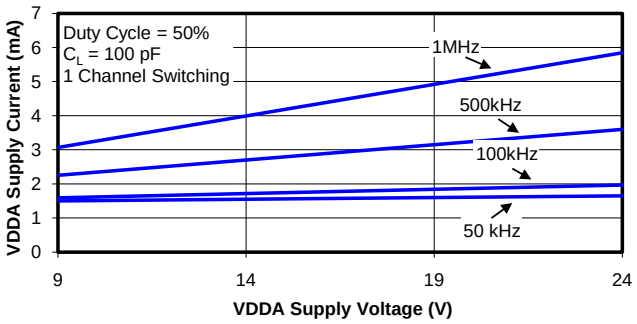


Figure 13. Supply Current vs. Supply Voltage

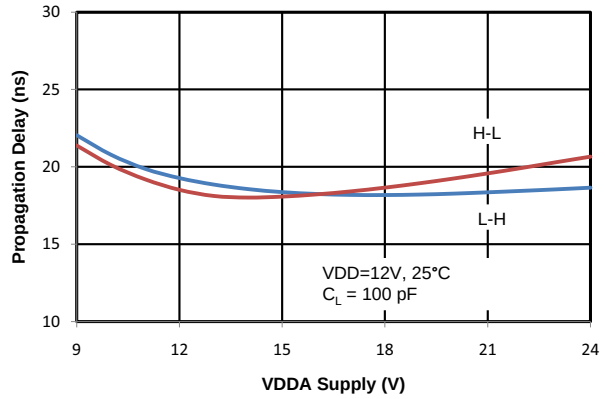


Figure 11. Propagation Delay vs. Supply Voltage

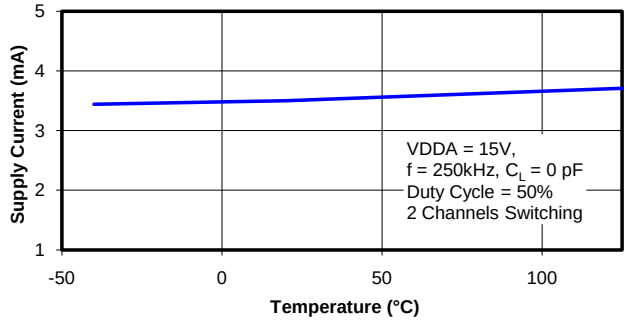


Figure 14. Supply Current vs. Temperature

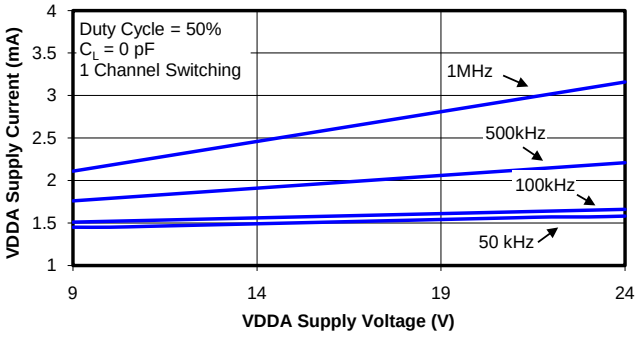


Figure 12. Supply Current vs. Supply Voltage

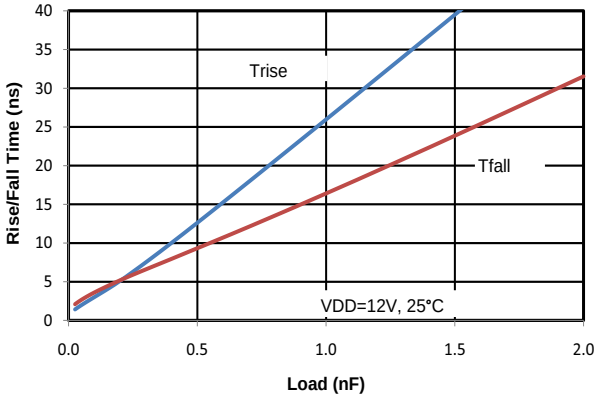


Figure 15. Rise/Fall Time vs. Load

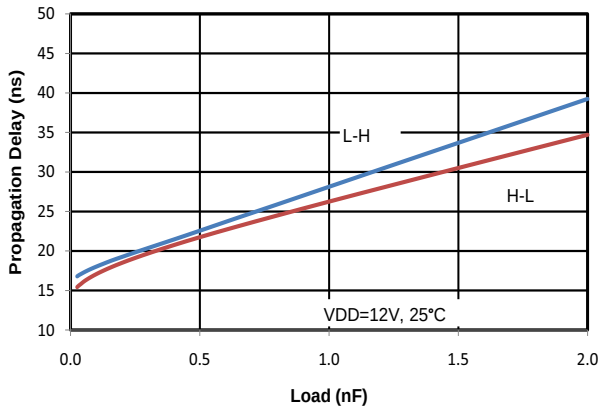


Figure 16. Propagation Delay vs. Load

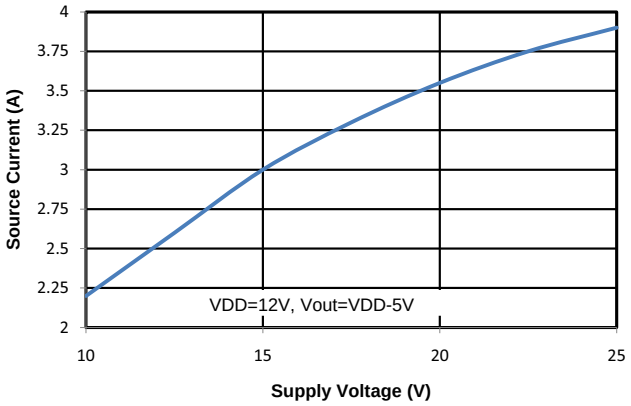


Figure 19. Output Source Current vs. Supply Voltage

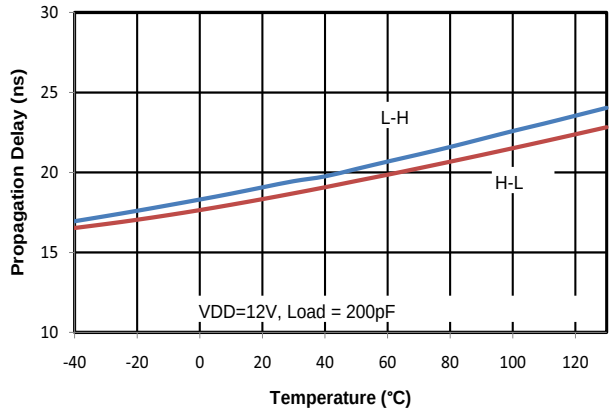


Figure 17. Propagation Delay vs. Temperature

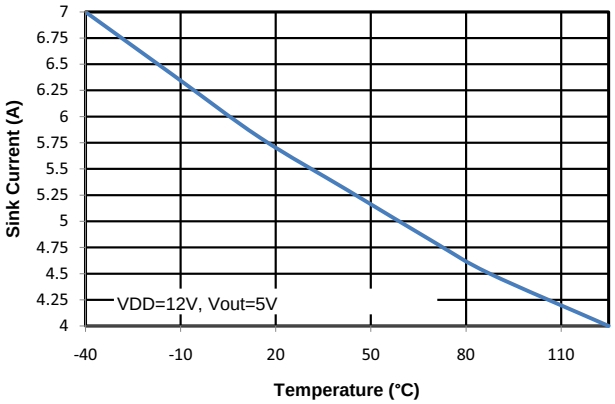


Figure 20. Output Sink Current vs. Temperature

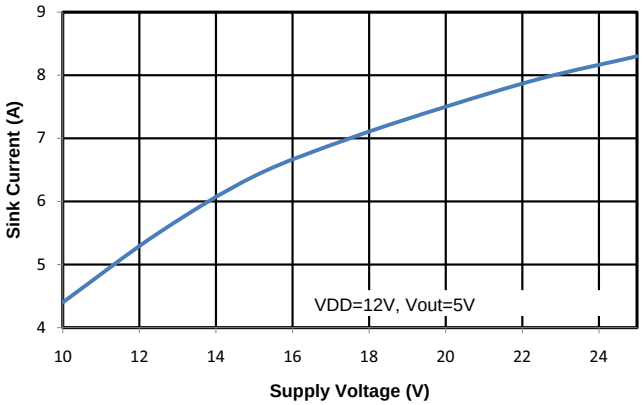


Figure 18. Output Sink Current vs. Supply Voltage

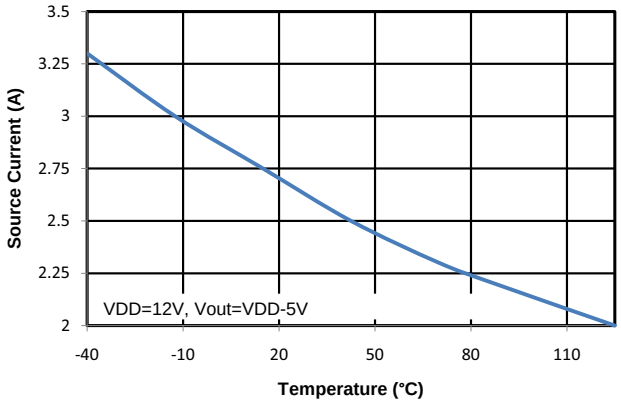


Figure 21. Output Source Current vs. Temperature

4. Typical Operating Characteristics (4.0 Amp)

The typical performance characteristics depicted in Figures 22 through 33 are for information purposes only. Refer to Table 1 on page 6 for actual specification limits.

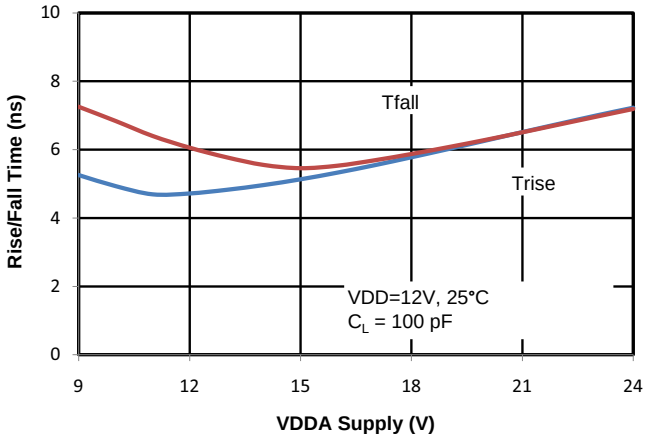


Figure 22. Rise/Fall Time vs. Supply Voltage

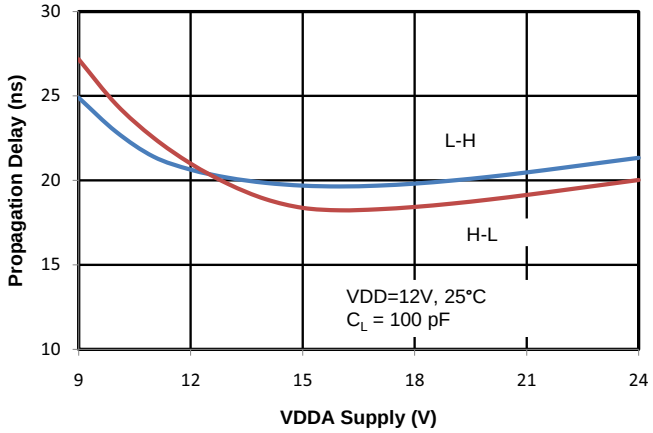


Figure 23. Propagation Delay vs. Supply Voltage

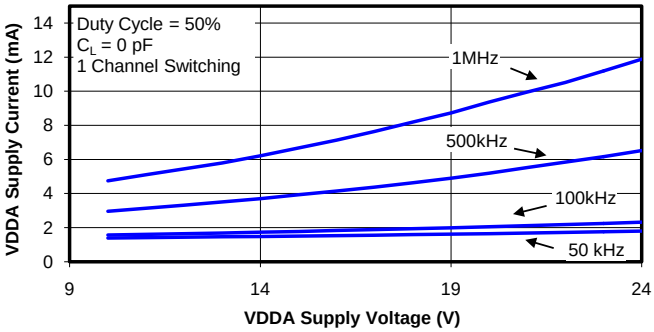


Figure 24. Supply Current vs. Supply Voltage

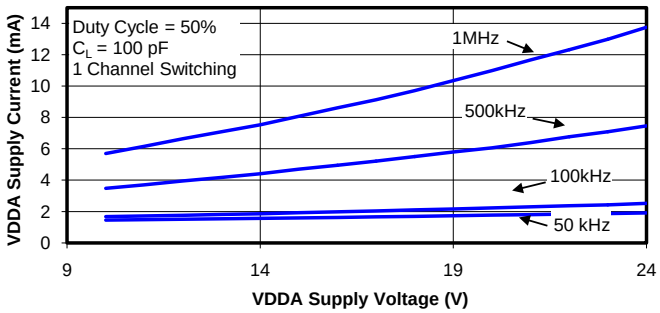


Figure 25. Supply Current vs. Supply Voltage

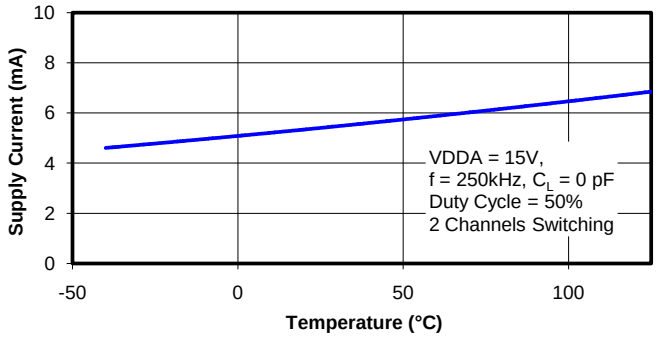


Figure 26. Supply Current vs. Temperature

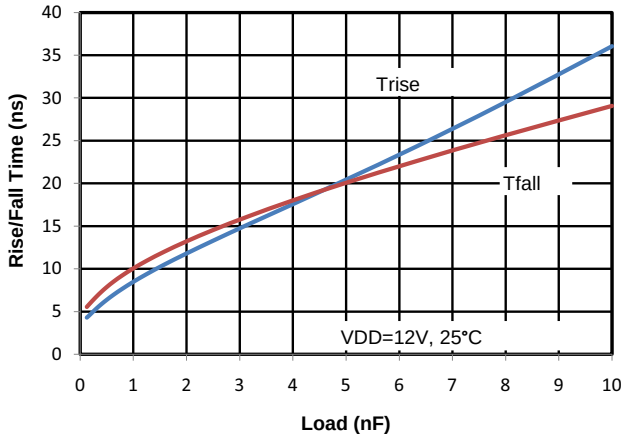


Figure 27. Rise/Fall Time vs. Load

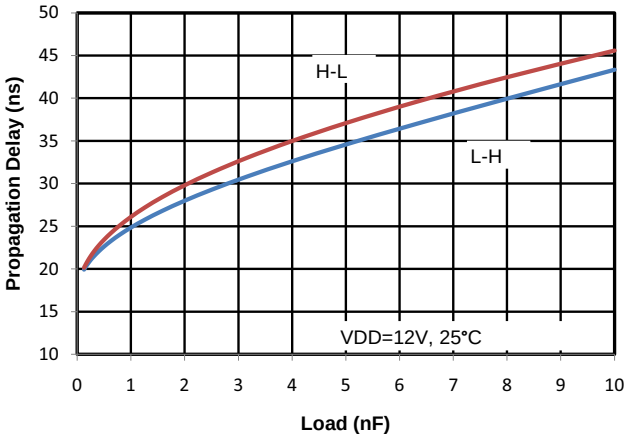


Figure 28. Propagation Delay vs. Load

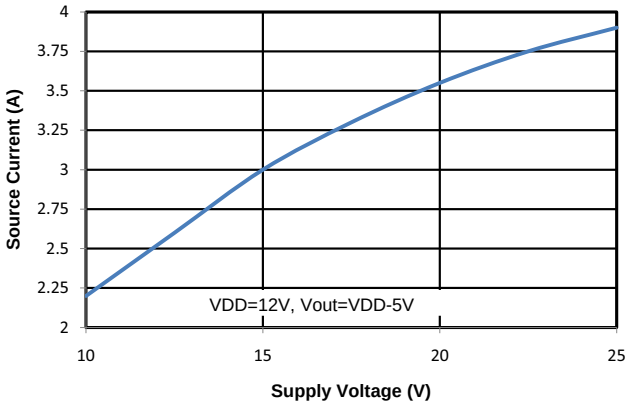


Figure 31. Output Source Current vs. Supply Voltage

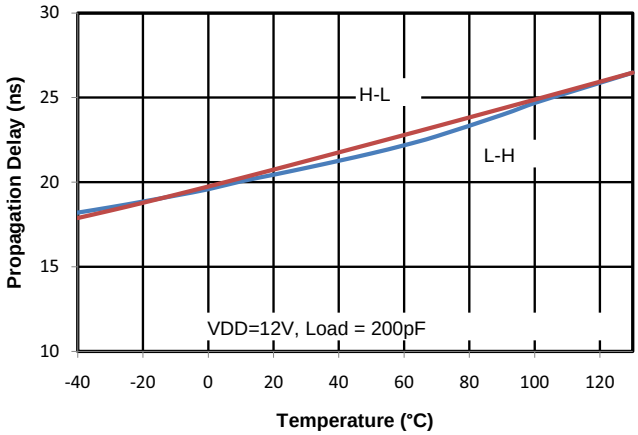


Figure 29. Propagation Delay vs. Temperature

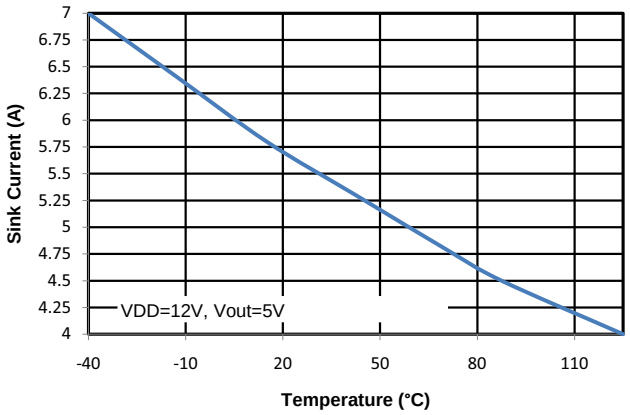


Figure 32. Output Sink Current vs. Temperature

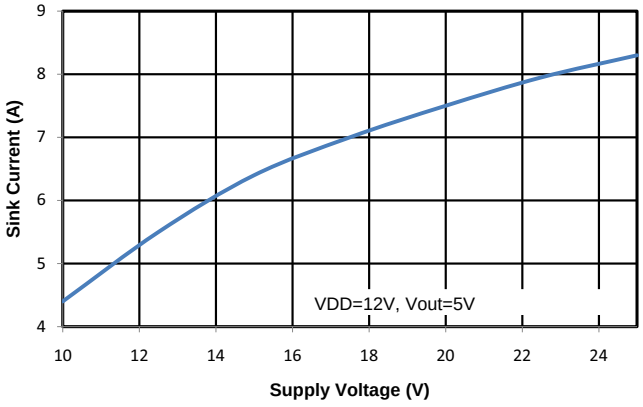


Figure 30. Output Sink Current vs. Supply Voltage

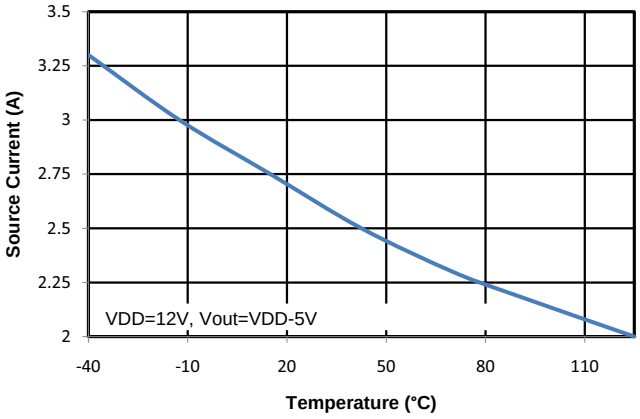


Figure 33. Output Source Current vs. Temperature

5. Application Information

The Si823x family of isolated drivers consists of high-side, low-side, and dual driver configurations.

5.1. Products

Table 9 shows the configuration and functional overview for each product in this family.

Table 9. Si823x Family Overview

Part Number	Configuration	Overlap Protection	Programmable Dead Time	Inputs	Peak Output Current (A)
Si8230	High-Side/Low-Side	✓	✓	VIA, VIB	0.5
Si8231	High-Side/Low-Side	✓	✓	PWM	0.5
Si8232	Dual Driver	—	—	VIA, VIB	0.5
Si8233	High-Side/Low-Side	✓	✓	VIA, VIB	4.0
Si8234	High-Side/Low-Side	✓	✓	PWM	4.0
Si8235/6	Dual Driver	—	—	VIA, VIB	4.0

5.2. Device Behavior

Table 10 contains truth tables for the Si8230/3, Si8231/4, and Si8232/5/6 families.

Table 10. Si823x Family Truth Table*

Si8230/3 (High-Side/Low-Side) Truth Table						
Inputs		VDDI State	Disable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	L	L	L	Output transition occurs after internal dead time expires.
L	H	Powered	L	L	H	Output transition occurs after internal dead time expires.
H	L	Powered	L	H	L	Output transition occurs after internal dead time expires.
H	H	Powered	L	L	L	Invalid state. Output transition occurs after internal dead time expires.
X	X	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.
Si8231/4 (PWM Input High-Side/Low-Side) Truth Table						
PWM Input		VDDI State	Disable	Output		Notes
				VOA	VOB	
H		Powered	L	H	L	Output transition occurs after internal dead time expires.
L		Powered	L	L	H	Output transition occurs after internal dead time expires.
X		Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X		Powered	H	L	L	Device is disabled.

***Note:** This truth table assumes VDDA and VDDB are powered. If VDDA or VDDB power is lost, the respective output state (VOA or VOB) is undetermined.

Table 10. Si823x Family Truth Table* (Continued)

Si8232/5/6 (Dual Driver) Truth Table						
Inputs		**VDDI State**	**Disable**	**Output**		**Notes**
VIA	**VIB**			**VOA**	**VOB**	
L	L	Powered	L	L	L	Output transition occurs immediately (no internal dead time).
L	H	Powered	L	L	H	Output transition occurs immediately (no internal dead time).
H	L	Powered	L	H	L	Output transition occurs immediately (no internal dead time).
H	H	Powered	L	H	H	Output transition occurs immediately (no internal dead time).
X	X	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.

***Note:** This truth table assumes VDDA and VDDB are powered. If VDDA or VDDB power is lost, the respective output state (VOA or VOB) is undetermined.

5.3. Power Supply Connections

Isolation requirements mandate individual supplies for VDDI, VDDA, and VDDB. The decoupling caps for these supplies must be placed as close to the VDD and GND pins of the Si823x as possible. The optimum values for these capacitors depend on load current and the distance between the chip and the regulator that powers it. Low effective series resistance (ESR) capacitors, such as Tantalum, are recommended.

5.4. Power Dissipation Considerations

Proper system design must assure that the Si823x operates within safe thermal limits across the entire load range. The Si823x total power dissipation is the sum of the power dissipated by bias supply current, internal switching losses, and power delivered to the load. Equation 1 shows total Si823x power dissipation. In a non-overlapping system, such as a high-side/low-side driver, n = 1. For a dual driver with each driver having an independent load, n can have a maximum value of 2, corresponding to a 100% overlap between the two outputs.

$$P_D = V_{DDI}I_{DDI} + 2(V_{DDO}I_{QOUT} + C_{int}V_{DDO}^2F) + 2n(C_LV_{DDO}^2F)$$

where:

P_D is the total Si823x device power dissipation (W)

I_{DDI} is the input-side maximum bias current (3 mA)

I_{QOUT} is the driver die maximum bias current (2.5 mA)

C_{int} is the internal parasitic capacitance (75 pF for the 0.5 A driver and 370 pF for the 4.0 A driver)

V_{DDI} is the input-side VDD supply voltage (4.5 to 5.5 V)

V_{DDO} is the driver-side supply voltage (10 to 24 V)

F is the switching frequency (Hz)

n is the overlap constant (max value = 2)

Equation 1.

The maximum power dissipation allowable for the Si823x is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2:

$$P_{Dmax} \leq \frac{T_{jmax} - T_A}{\theta ja}$$

where:

P_{Dmax} = Maximum Si823x power dissipation (W)

T_{jmax} = Si823x maximum junction temperature (145 °C)

T_A = Ambient temperature (°C)

θja = Si823x junction-to-air thermal resistance (105 °C/W)

F = Si823x switching frequency (Hz)

Equation 2.

Substituting values for PDMAX TjMAX, TA, and θ_{ja} into Equation 2 results in a maximum allowable total power dissipation of 1.1 W. Maximum allowable load is found by substituting this limit and the appropriate datasheet values from Table 1 on page 6 into Equation 1 and simplifying. The result is Equation 3 (0.5 A driver) and Equation 4 (4.0 A driver), both of which assume VDDI = 5 V and VDDA = VDDB = 18 V.

$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{F} - 7.5 \times 10^{-11}$$

Equation 3.

$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{F} - 3.7 \times 10^{-10}$$

Equation 4.

Equation 1 and Equation 2 are graphed in Figure 34 where the points along the load line represent the package dissipation-limited value of CL for the corresponding switching frequency.

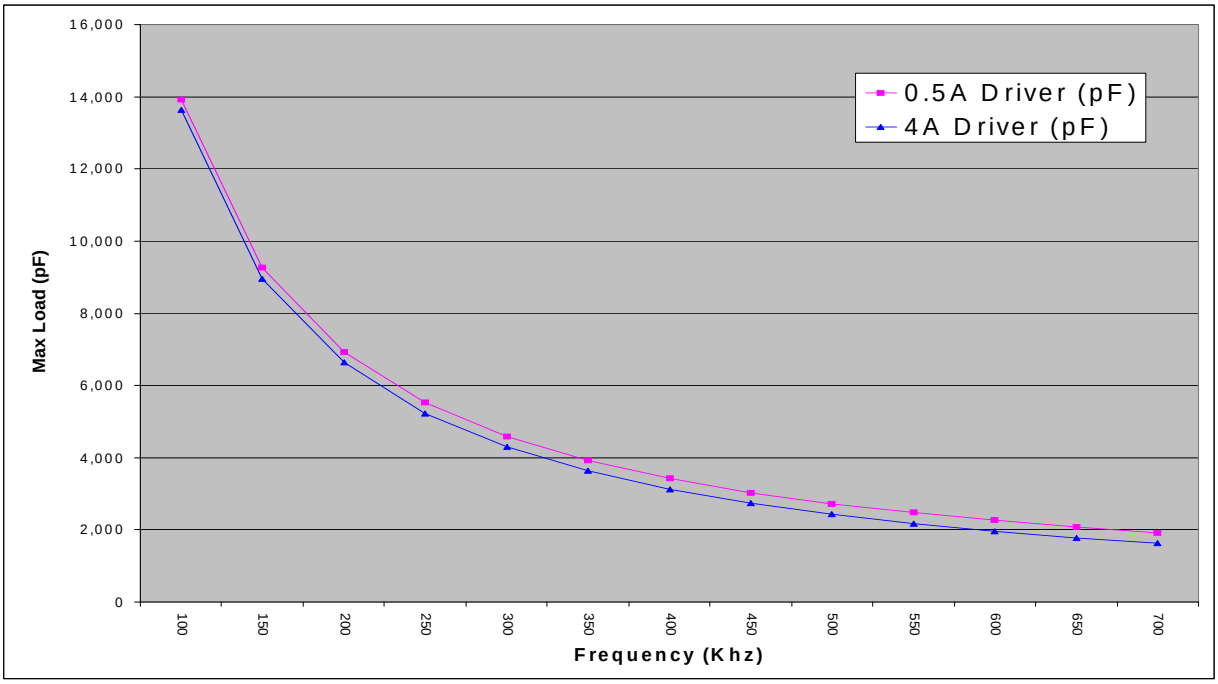


Figure 34. Max Load vs. Switching Frequency

5.5. Layout Considerations

It is most important to minimize ringing in the drive path and noise on the Si823x VDD lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si823x as close to the device it is driving as possible. In addition, the VDD supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and VDD planes for power devices and small signal components provides the best overall noise performance.

5.6. Device Operation

Device behavior during start-up, normal operation and shutdown is shown in Figure 35, where UVLO+ and UVLO- are the positive-going and negative-going thresholds respectively. Note that outputs VOA and VOB default low when input side power supply (VDDI) is not present.

5.6.1. Device Startup

Outputs VOA and VOB are held low during power-up until VDD is above the UVLO threshold for time period tSTART. Following this, the outputs follow the states of inputs VIA and VIB.

5.6.2. Under Voltage Lockout

Under Voltage Lockout (UVLO) is provided to prevent erroneous operation during device startup and shutdown or when VDD is below its specified operating circuits range. The input (control) side, Driver A and Driver B, each have their own under voltage lockout monitors.

The Si823x input side enters UVLO when VDDI $\leq$ $VDDI_{UV-}$, and exits UVLO when VDDI > $VDDI_{UV+}$. The driver outputs, VOA and VOB, remain low when the input side of the Si823x is in UVLO and their respective VDD supply (VDDA, VDDB) is within tolerance. Each driver output can enter or exit UVLO independently. For example, VOA unconditionally enters UVLO when VDDA falls below $VDDA_{UV-}$ and exits UVLO when VDDA rises above $VDDA_{UV+}$.

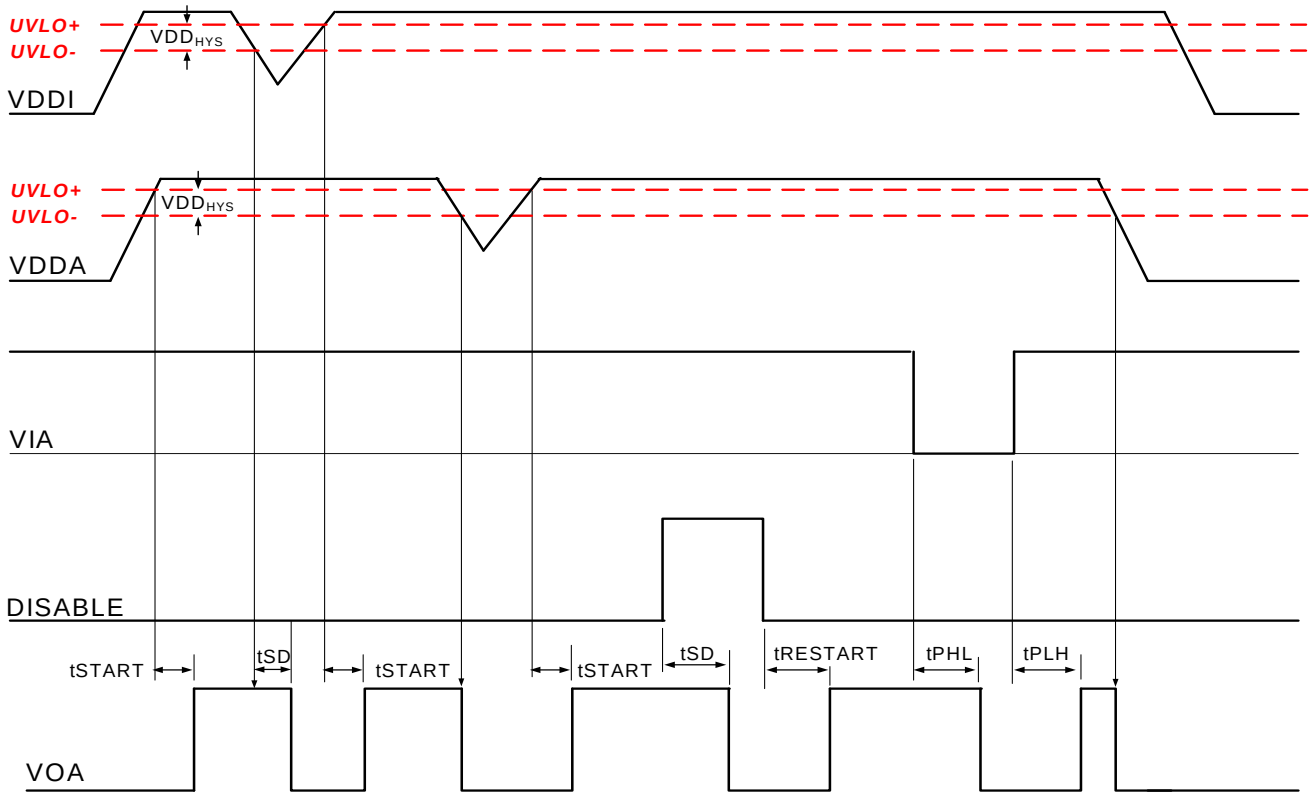


Figure 35. Device Behavior during Normal Operation and Shutdown

5.6.3. Under Voltage Lockout (UVLO)

The UVLO circuit unconditionally drives VO low when VDD is below the lockout threshold. Referring to Figures 36 through 39, upon power up, the Si823x is maintained in UVLO until VDD rises above VDD_{UV+}. During power down, the Si823x enters UVLO when VDD falls below the UVLO threshold plus hysteresis (i.e., VDD ≤ VDD_{UV+} – VDD_{HYS}).

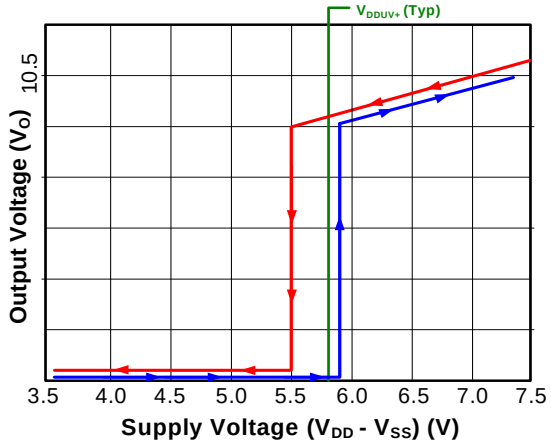


Figure 36. Si823x UVLO Response (5 V)

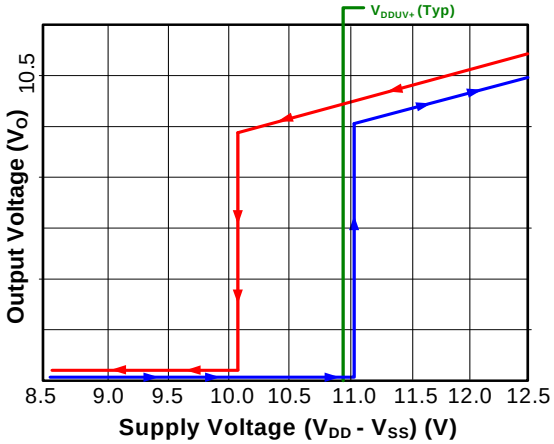


Figure 38. Si823x UVLO Response (10 V)

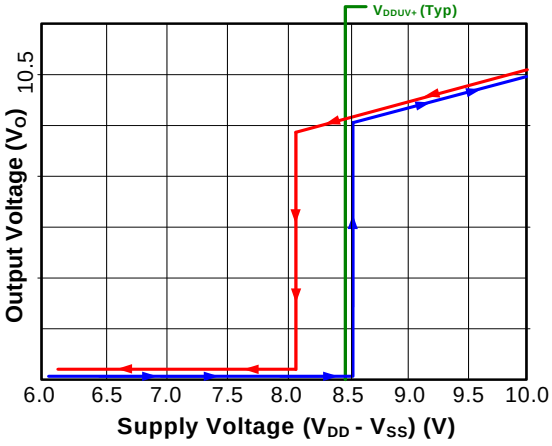


Figure 37. Si823x UVLO Response (8 V)

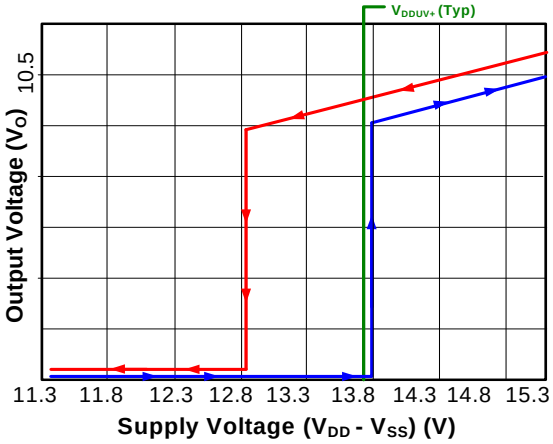


Figure 39. Si823x UVLO Response (12.5 V)

5.6.4. Control Inputs

VIA, VIB, and PWM inputs are high-true, TTL level-compatible logic inputs. A logic high signal on VIA or VIB causes the corresponding output to go high. For PWM input versions (Si8231/4), VOA is high and VOB is low when the PWM input is high, and VOA is low and VOB is high when the PWM input is low.

5.6.5. Disable Input

When brought high, the DISABLE input unconditionally drives VOA and VOB low regardless of the states of VIA and VIB. Device operation terminates within tSD after DISABLE = V_{IH} and resumes within tRESTART after DISABLE = V_{IL}. The DISABLE input has no effect if VDDI is below its UVLO level (i.e. VOA, VOB remain low).

5.7. Programmable Dead Time and Overlap Protection

All high-side/low-side drivers (Si8230/1/3/4) include programmable overlap protection to prevent outputs VOA and VOB from being high at the same time. These devices also include programmable dead time, which adds a user-programmable delay between transitions of VOA and VOB (Figure 26.A). When enabled, dead time is present on all transitions, even after overlap recovery (Figure 26.B). The amount of dead time delay (DT) is programmed by a single resistor (RDT) connected from the DT input to ground per Equation 5. Note that the dead time pin can be tied to VDDI or left floating to provide a nominal dead time at approximately 400 ps.

$$DT \approx 10 \times RDT$$

where:

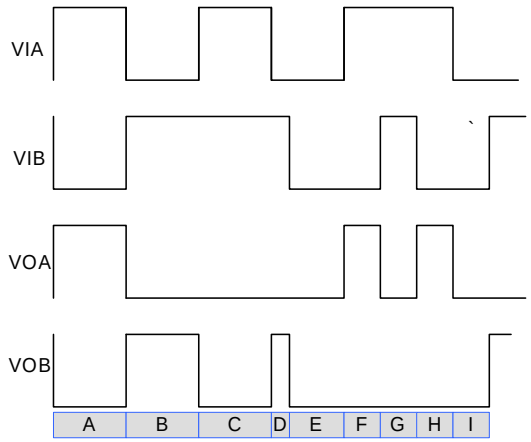
DT= dead time (ns)

and

RDT= dead time programming resistor (kΩ)

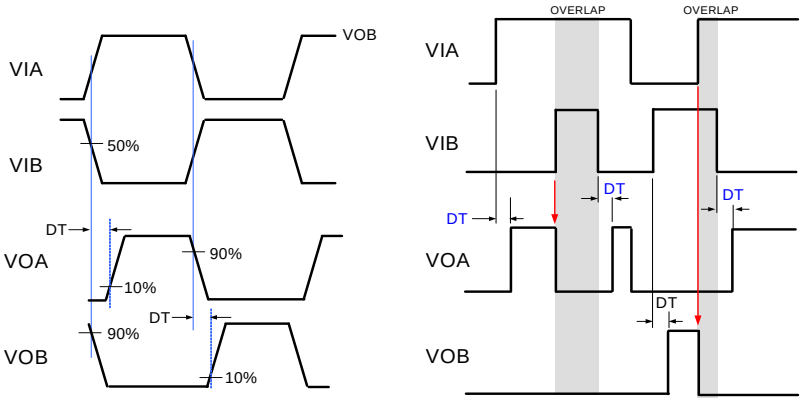
Equation 5.

The device driving VIA and VIB should provide a minimum dead time of TDD to avoid activating overlap protection. Input/output timing waveforms for the two-input drivers are shown in Figure 40, and dead time waveforms are shown in Figure 41.



Ref	Description
A	Normal operation: VIA high, VIB low.
B	Normal operation: VIB high, VIA low.
C	Contention: VIA = VIB = high.
D	Recovery from contention: VIA transitions low.
E	Normal operation: VIA = VIB = low.
F	Normal operation: VIA high, VIB low.
G	Contention: VIA = VIB = high.
H	Recovery from contention: VIB transitions low.
I	Normal operation: VIB transitions high.

Figure 40. Input / Output Waveforms for High-Side / Low-Side Two-Input Drivers



A. Typical Dead Time Operation

B. Dead Time Operation During Overlap

Figure 41. Dead Time Waveforms for High-Side/Low-Side Two-Input Drivers

6. RF Radiated Emissions

The Si823x family uses a RF carrier frequency of approximately 700 MHz. This results in a small amount of radiated emissions at this frequency and its harmonics. The radiation is not from the IC but, rather, is due to a small amount of RF energy driving the isolated ground planes which can act as a dipole antenna.

The unshielded Si8230 evaluation board passes FCC Class B (Part 15) requirements. Table 11 shows measured emissions compared to FCC requirements. Note that the data reflects worst-case conditions where all inputs are tied to logic 1 and the RF transmitters are fully active.

Radiated emissions can be reduced if the circuit board is enclosed in a shielded enclosure or if the PCB is a less efficient antenna.

Table 11. Radiated Emissions

Frequency (MHz)	Measured (dBµV/m)	FCC Spec (dBµV/m)	Compared to Spec (dB)
712	29	37	–8
1424	39	54	–15
2136	42	54	–12
2848	43	54	–11
4272	44	54	–10
4984	44	54	–10
5696	44	54	–10

6.1. RF, Magnetic, and Common Mode Transient Immunity

The Si823x families have very high common mode transient immunity while transmitting data. This is typically measured by applying a square pulse with very fast rise/fall times between the isolated grounds. Measurements show no failures at 30 kV/µs (minimum). During a high surge event, the output may glitch low for up to 20–30 ns, but the output corrects immediately after the surge event.

The Si823x families pass the industrial requirements of CISPR24 for RF immunity of 10 V/m using an unshielded evaluation board. As shown in Figure 20, the isolated ground planes form a parasitic dipole antenna. The PCB should be laid-out to not act as an efficient antenna for the RF frequency of interest. RF susceptibility is also significantly reduced when the end system is housed in a metal enclosure, or otherwise shielded.

The Si823x digital isolator can be used in close proximity to large motors and various other magnetic-field producing equipment. In theory, data transmission errors can occur if the magnetic field is too large and the field is too close to the isolator. However, in actual use, the Si823x devices provide extremely high immunity to external magnetic fields and have been independently evaluated to withstand magnetic fields of at least 1000 A/m according to the IEC 61000-4-8 and IEC 61000-4-9 specifications.

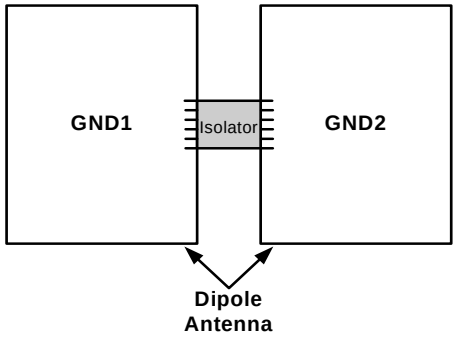


Figure 42. Dipole Antenna

7. Applications

The following examples illustrate typical circuit configurations using the Si823x.

7.1. High-Side / Low-Side Driver

Figure 43A shows the Si8230/3 controlled using the VIA and VIB input signals, and Figure 43B shows the Si8231/4 controlled by a single PWM signal.

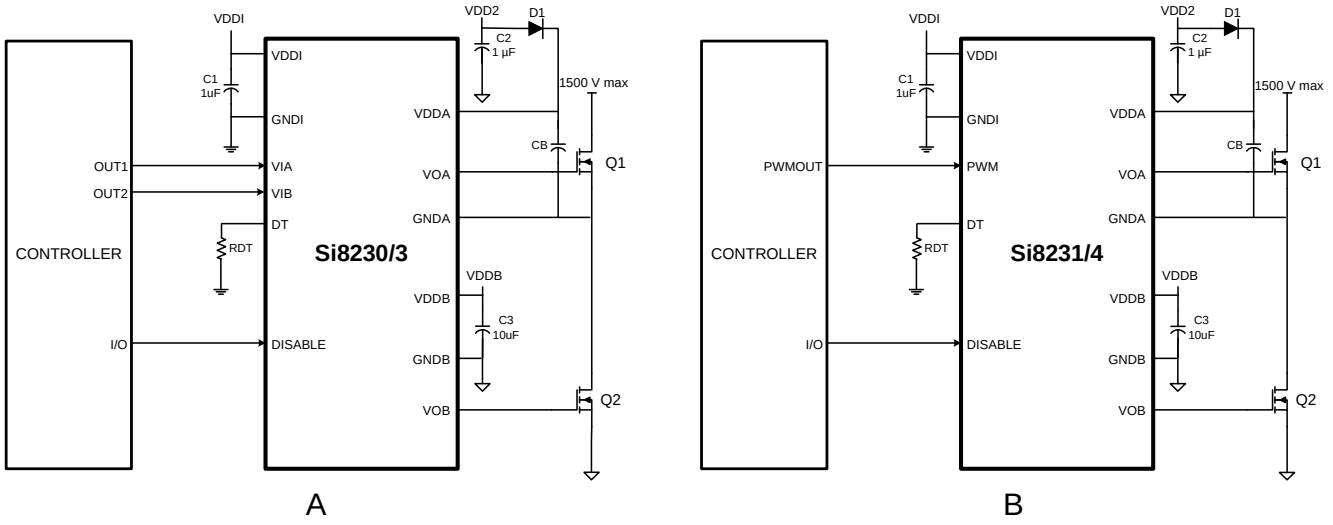


Figure 43. Si823x in Half-Bridge Application

For both cases, D1 and CB form a conventional bootstrap circuit that allows VOA to operate as a high-side driver for Q1, which has a maximum drain voltage of 1500 V. VOB is connected as a conventional low-side driver. Note that the input side of the Si823x requires VDD in the range of 4.5 to 5.5 V, while the VDDA and VDDB output side supplies must be between 6.5 and 24 V with respect to their respective grounds. The boot-strap start up time will depend on the CB cap chosen. VDD2 is usually the same as VDDB. Also note that the bypass capacitors on the Si823x should be located as close to the chip as possible. Moreover, it is recommended that 0.1 and 10 µF bypass capacitors be used to reduce high frequency noise and maximize performance.

7.2. Dual Driver

Figure 44 shows the Si823x configured as a dual driver. Note that the drain voltages of Q1 and Q2 can be referenced to a common ground or to different grounds with as much as 1500 V dc between them.

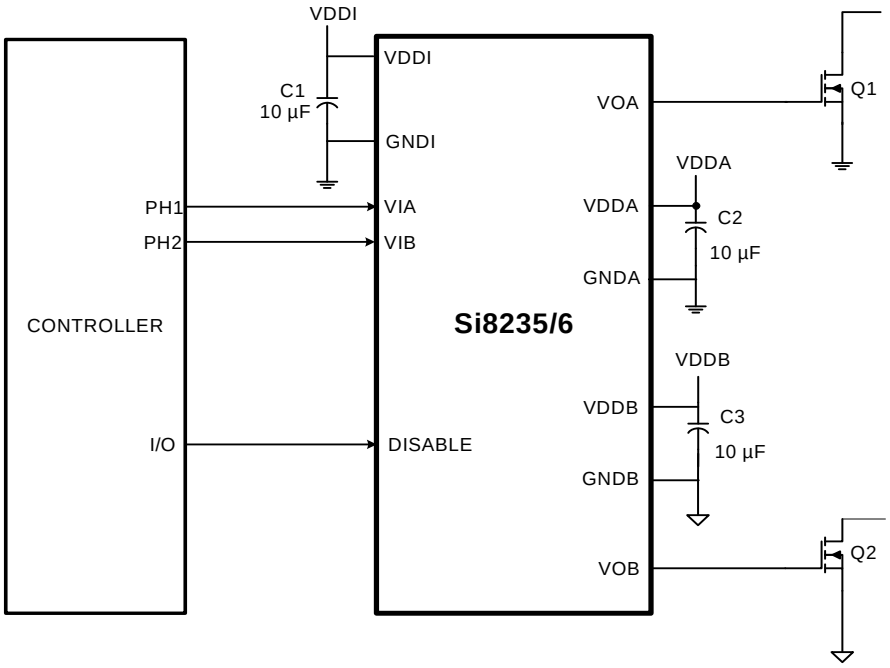


Figure 44. Si8235 in a Dual Driver Application

7.3. Dual Driver with Thermally Enhanced Package (Si8236)

The thermal pad of the Si8236 must be connected to a heat spreader to lower thermal resistance. Generally, the larger the thermal shield's area, the lower the thermal resistance. It is recommended that a thermal vias also be used to add mass to the shield. Vias generally have much more mass than the shield alone and consume less space, thus reducing thermal resistance more effectively. While the heat spreader is not generally a circuit ground, it is a good reference plane for the Si8236 and is also useful as a shield layer for EMI reduction.

With a 10mm^2 thermal plane on the outer layers (including 20 thermal vias), the thermal impedance of the Si8236 was measured at 50 °C/W. This is a significant improvement over the Si835 which does not include a thermal pad. The Si8235's thermal resistance was measured at 105 °C /W.

8. Pin Descriptions

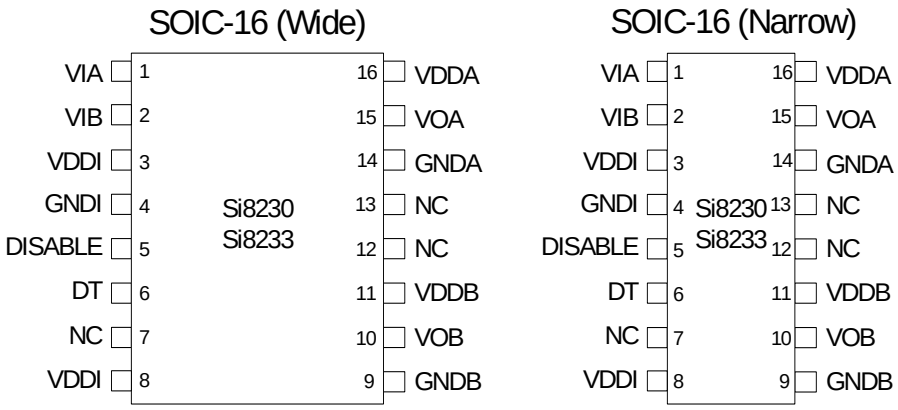


Table 12. Si8230/3 Two-Input HS/LS Isolated Driver (SOIC-16)

Pin	Name	Description
1	VIA	Non-inverting logic input terminal for Driver A.
2	VIB	Non-inverting logic input terminal for Driver B.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 1 ns dead time when connected to VDDI or left open (see "5.7.Programmable Dead Time and Overlap Protection" on page 26).
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output (low-side driver).
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

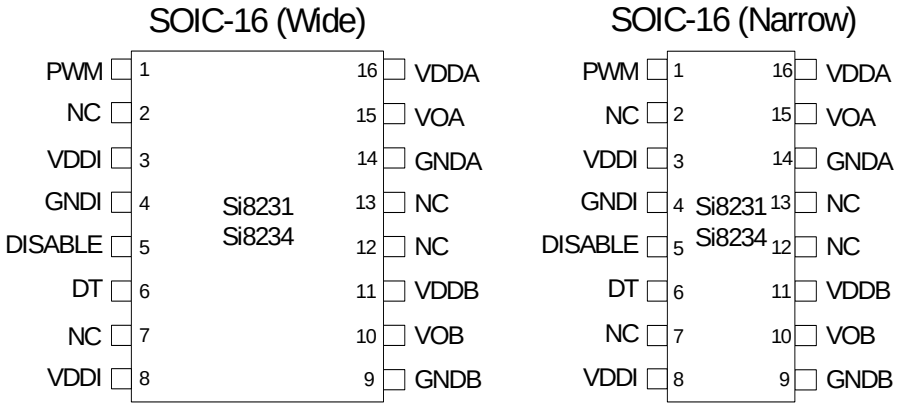


Table 13. Si8231/4 PWM Input HS/LS Isolated Driver (SOIC-16)

Pin	Name	Description
1	PWM	PWM input.
2	NC	No connection.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 1 ns dead time when connected to VDDI or left open (see "5.7.Programmable Dead Time and Overlap Protection" on page 26).
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for VOB driver output.
10	VOB	Driver B output (low-side driver).
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

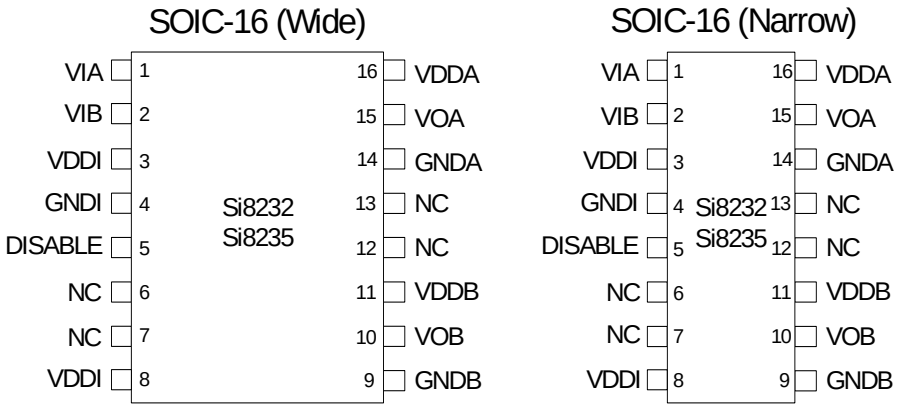


Table 14. Si8232/5 Dual Isolated Driver (SOIC-16)

Pin	Name	Description
1	VIA	Non-inverting logic input terminal for Driver A.
2	VIB	Non-inverting logic input terminal for Driver B.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	NC	No connection.
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for VOB driver output.
10	VOB	Driver B output.
11	VDDB	Driver output VOB power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver B output.
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

LGA-14 (5 x 5 mm)

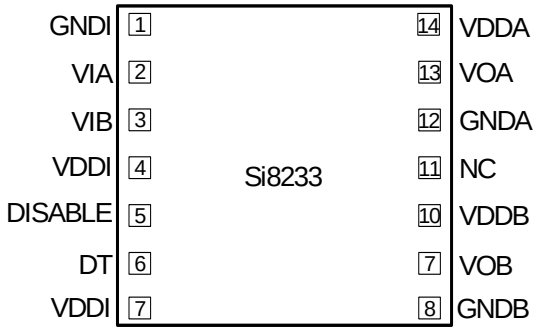


Table 15. Si8233 Two-Input HS/LS Isolated Driver (14 LD LGA)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
VIA	2	Non-inverting logic input terminal for Driver A.
VIB	3	Non-inverting logic input terminal for Driver B.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DT	6	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 1 ns dead time when connected to VDDI or left open (see"5.7.Programmable Dead Time and Overlap Protection" on page 26).
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

LGA-14 (5 x 5 mm)

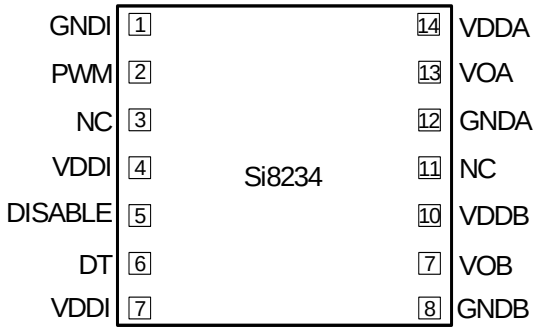


Table 16. Si8234 PWM Input HS/LS Isolated Driver (14 LD LGA)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
PWM	2	PWM input.
NC	3	No connection.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DT	6	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 1 ns dead time when connected to VDDI or left open (see "5.7.Programmable Dead Time and Overlap Protection" on page 26).
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

LGA-14 (5 x 5 mm)

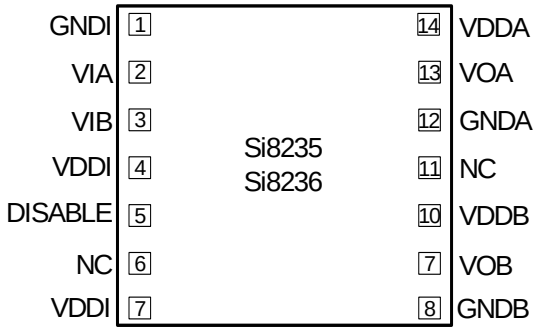
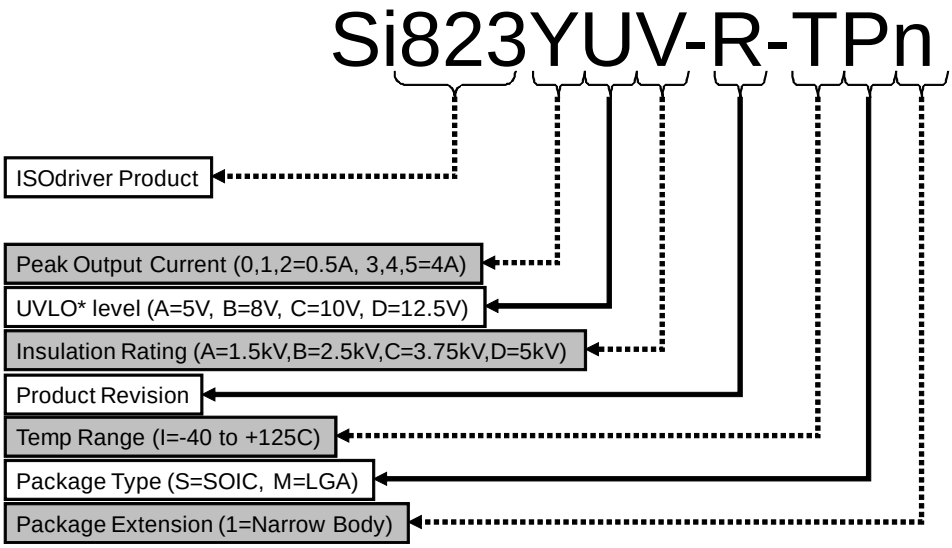


Table 17. Si8235/6 Dual Isolated Driver (14 LD LGA)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
VIA	2	Non-inverting logic input terminal for Driver A.
VIB	3	Non-inverting logic input terminal for Driver B.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
NC	6	No connection.
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

9. Ordering Guide

The ordering part number (OPN) naming convention is described in Figure 45. The currently available OPNs are listed in Table 18. The part number convention is not intended to imply that all possible device configuration options and their corresponding ordering part numbers (OPN) will be available or are included in the ordering guide table. However, if there is a specific device configuration of interest that is currently not listed in the ordering guide table, contact your local Silicon Labs sales representative, or go to the Silicon Labs Technical Support web page at https://www.silabs.com/support/pages/contacttechnicalsupport.aspx and register to submit a request for your specific device configuration and OPN. Ordering part number options for 10 V and 12.5 V UVLO will be made available only by request.



Note: UVLO = Under Voltage Lock Out for VDDA, VDDB.

Figure 45. ISODriver OPN Naming Convention

Table 18. Ordering Part Numbers

Ordering Part Number (OPN)	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Temperature Range	Package Type	Legacy Ordering Part Number (OPN) 2.5 kV Only
Wide Body (WB) Package Options								
Si8230BB-B-IS	VIA, VIB	High Side/ Low Side	0.5 A	8 V	2.5 kVrms	–40 to +125 °C	SOIC-16 Wide Body	Si8230-A-IS
Si8231BB-B-IS	PWM	High Side/ Low Side						Si8231-A-IS
Si8232BB-B-IS	VIA,VIB	Dual Driver						Si8232-A-IS
Si8233BB-C-IS	VIA,VIB	High Side/ Low Side	4.0 A	8 V				Si8233-B-IS
Si8234BB-C-IS	PWM	High Side/ Low Side						Si8234-B-IS
Si8235BB-C-IS	VIA,VIB	Dual Driver						Si8235-B-IS
Narrow Body (NB) Package Options								
Si8230BB-B-IS1	VIA,VIB	High Side/ Low Side	0.5 A	8 V	2.5 kVrms	–40 to +125 °C	SOIC-16 Narrow Body	N/A
Si8231BB-B-IS1	PWM	High Side/ Low Side						
Si8232BB-B-IS1	VIA,VIB	Dual Driver						
Si8233BB-C-IS1	VIA,VIB	High Side/ Low Side	4.0 A	8 V				
Si8234BB-C-IS1	PWM	High Side/ Low Side						
Si8235BB-C-IS1	VIA,VIB	Dual Driver						

Note: All packages are RoHS-compliant.
Moisture sensitivity level is MSL3 for wide-body SOIC-16 and 14-LD LGA packages and MSL2A for narrow-body SOIC-16 packages with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

Table 18. Ordering Part Numbers (Continued)

Ordering Part Number (OPN)	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Temperature Range	Package Type	Legacy Ordering Part Number (OPN) 2.5 kV Only
LGA Package Options								
Si8233BB-C-IM	VIA,VIB	High Side/ Low Side	4.0 A	8 V	2.5 kVrms	–40 to +125 °C	LGA-14 5x5 mm	Si8233-B-IM
Si8234BB-C-IM	PWM	High Side/ Low Side						Si8234-B-IM
Si8235BB-C-IM	VIA,VIB	Dual Driver						Si8235-B-IM
Si8235AB-C-IM	VIA,VIB	Dual Driver		5 V				N/A
Si8236BA-C-IM	VIA, VIB	Dual Driver		8 V	1.5 kVrms		LGA-14 5x5 mm with Thermal Pad	Si8236-B-IM
Si8236AA-C-IM	VIA,VIB	Dual Driver		5 V				
5 kV Ordering Options								
Si8230BD-B-IS	VIA, VIB	High Side/ Low Side	0.5 A	8 V	5.0 kVrms	–40 to +125 °C	SOIC-16 Wide Body	N/A
Si8231BD-B-IS	PWM	High Side/ Low Side						
Si8232BD-B-IS	VIA, VIB	Dual Driver						
Si8233BD-C-IS	VIA, VIB	High Side/ Low Side	4.0 A					
Si8234BD-C-IS	PWM	High Side/ Low Side						
Si8235BD-C-IS	VIA, VIB	Dual Driver						

Note: All packages are RoHS-compliant.
Moisture sensitivity level is MSL3 for wide-body SOIC-16 and 14-LD LGA packages and MSL2A for narrow-body SOIC-16 packages with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.

10. Package Outline: 16-Pin Wide Body SOIC

Figure 46 illustrates the package details for the Si823x in a 16-Pin Wide Body SOIC. Table 19 lists the values for the dimensions shown in the illustration.

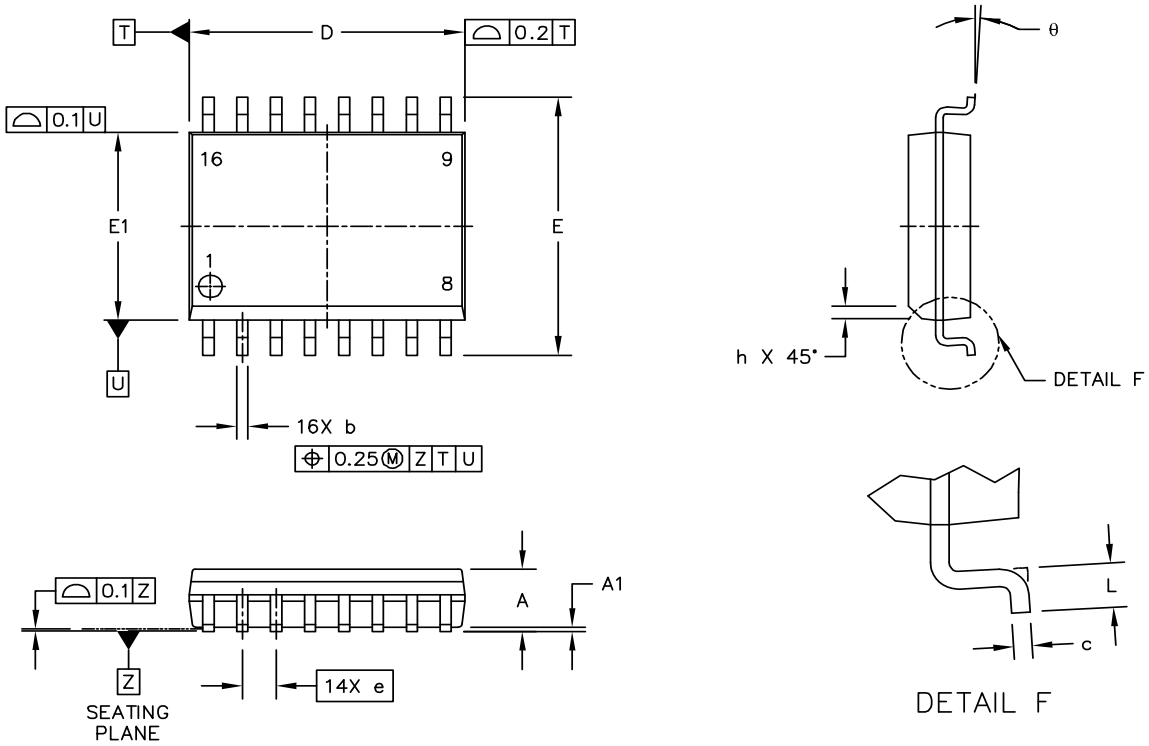


Figure 46. 16-Pin Wide Body SOIC

Table 19. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.1	0.3
D	10.3 BSC	
E	10.3 BSC	
E1	7.5 BSC	
b	0.31	0.51
c	0.20	0.33
e	1.27 BSC	
h	0.25	0.75
L	0.4	1.27
θ	0°	7°

11. Land Pattern: Wide-Body SOIC

Figure 47 illustrates the recommended land pattern details for the Si823x in a 16-pin wide-body SOIC. Table 20 lists the values for the dimensions shown in the illustration.

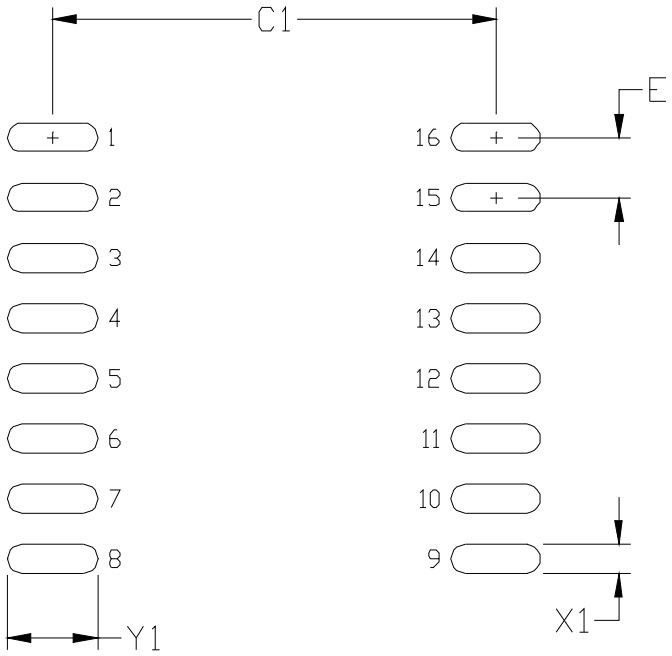


Figure 47. 16-Pin SOIC Land Pattern

Table 20. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

12. Package Outline: Narrow Body SOIC

Figure 48 illustrates the package details for the Si823x in a 16-pin narrow-body SOIC (SO-16). Table 21 lists the values for the dimensions shown in the illustration.

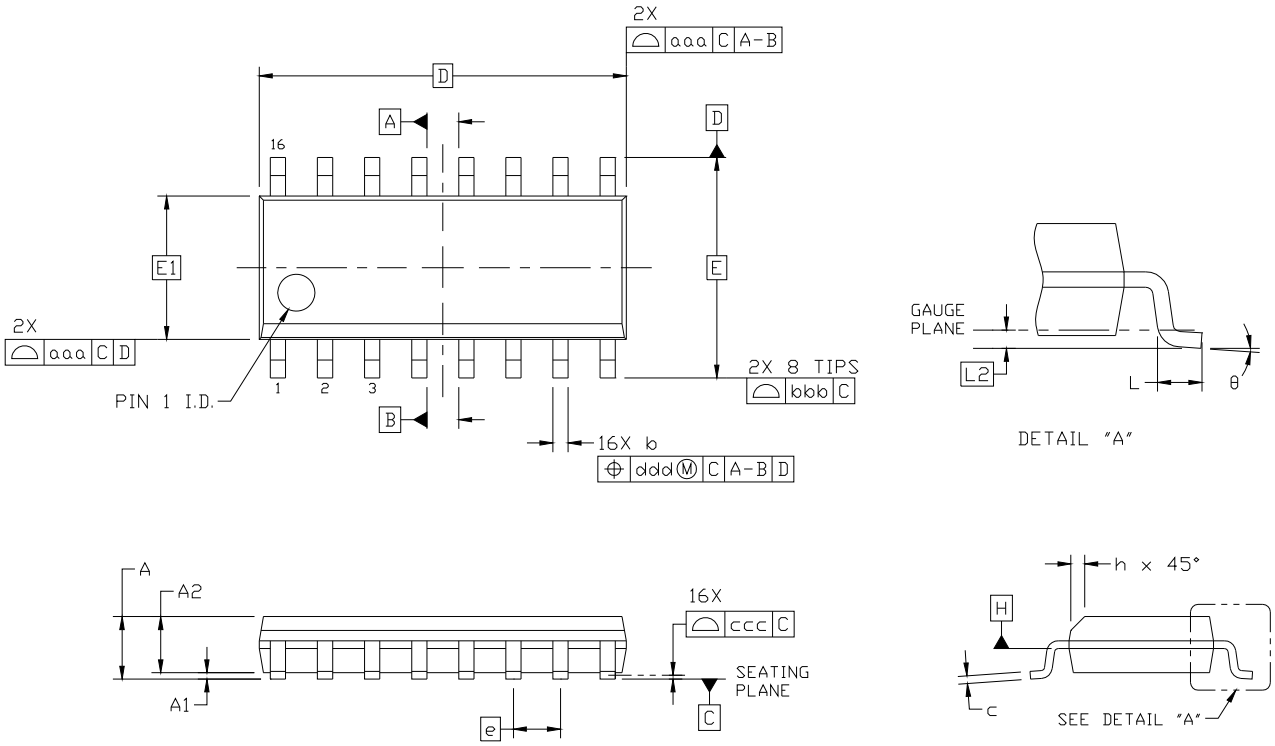


Figure 48. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 21. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.25 BSC	

Table 21. Package Diagram Dimensions (Continued)

h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

13. Land Pattern: Narrow Body SOIC

Figure 49 illustrates the recommended land pattern details for the Si823x in a 16-pin narrow-body SOIC. Table 22 lists the values for the dimensions shown in the illustration.

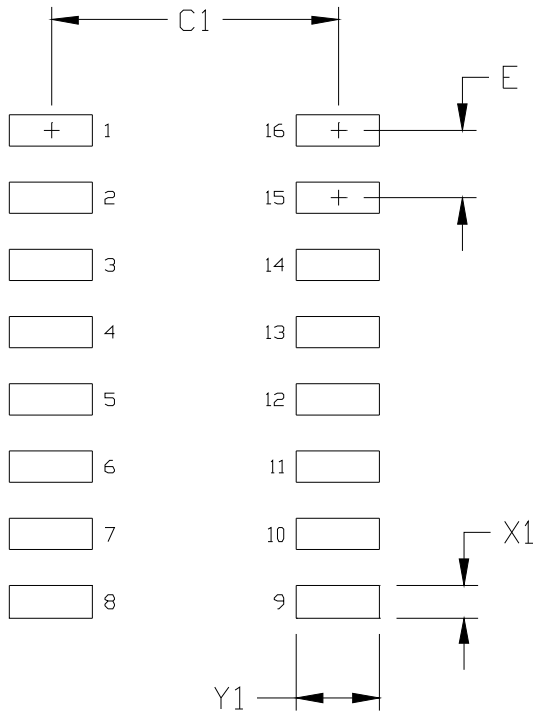


Figure 49. 16-Pin Narrow Body SOIC PCB Land Pattern

Table 22. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

14. Package Outline: 14 LD LGA (5 x 5 mm)

Figure 50 illustrates the package details for the Si823x in an LGA outline. Table 23 lists the values for the dimensions shown in the illustration.

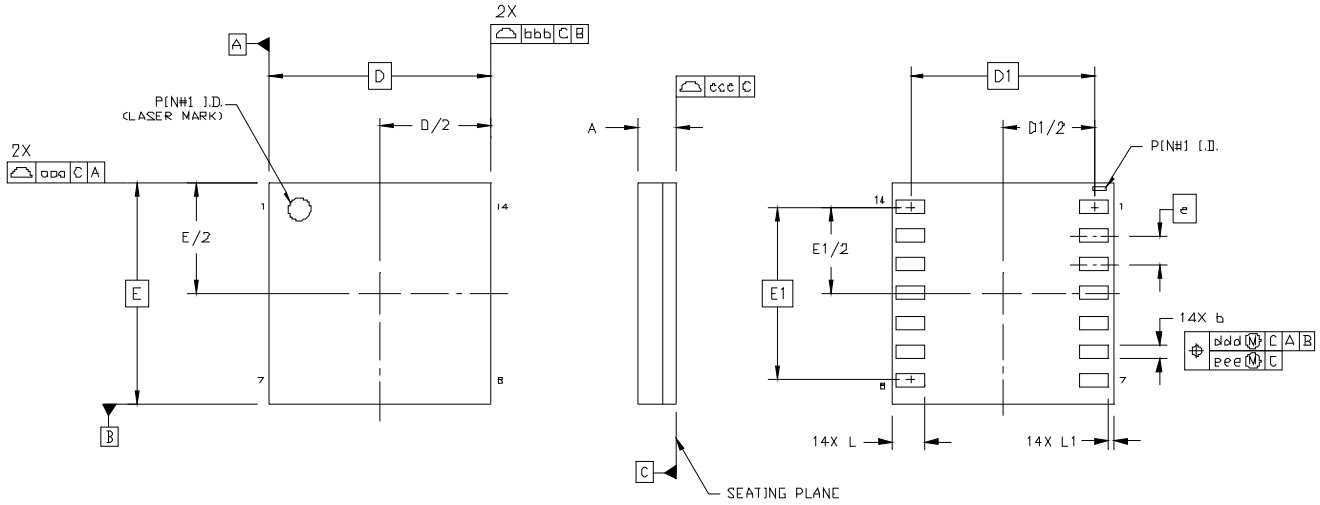


Figure 50. Si823x LGA Outline

Table 23. Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.74	0.84	0.94
b	0.25	0.30	0.35
D	5.00 BSC		
D1	4.15 BSC		
e	0.65 BSC		
E	5.00 BSC		
E1	3.90 BSC		
L	0.70	0.75	0.80
L1	0.05	0.10	0.15
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.15
eee	—	—	0.08

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

15. Land Pattern: 14 LD LGA

Figure 51 illustrates the recommended land pattern details for the Si823x in a 14-pin LGA. Table 24 lists the values for the dimensions shown in the illustration.

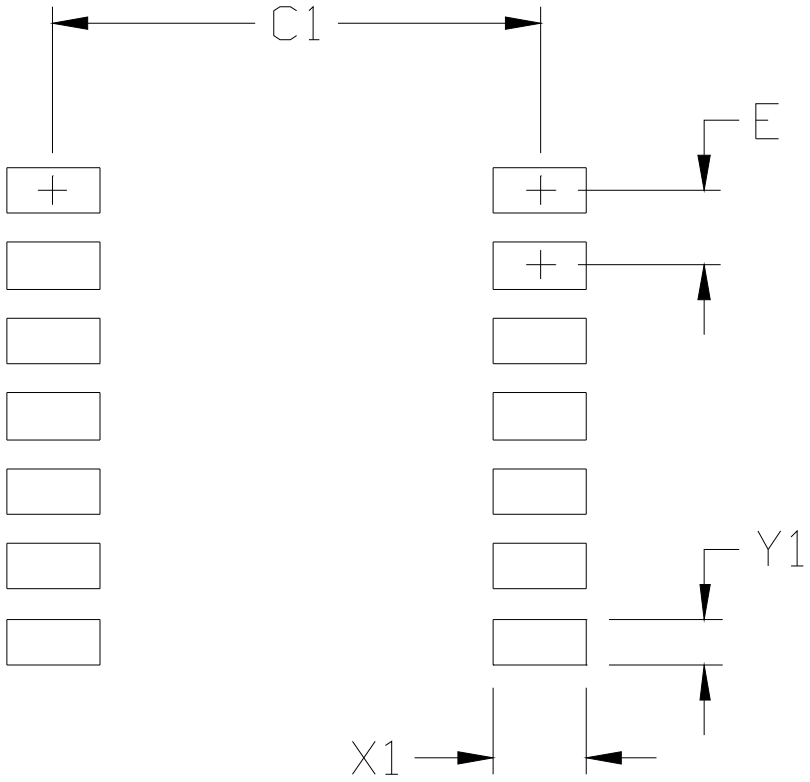


Figure 51. 14-Pin LGA Land Pattern

Table 24. 14-Pin LGA Land Pattern Dimensions

Dimension	(mm)
C1	4.20
E	0.65
X1	0.80
Y1	0.40

Notes:

General:

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design:

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design:

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly:

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

16. Package Outline: 14 LD LGA with Thermal Pad (5 x 5 mm)

Figure 52 illustrates the package details for the Si8236 ISOdriver in an LGA outline. Table 25 lists the values for the dimensions shown in the illustration.

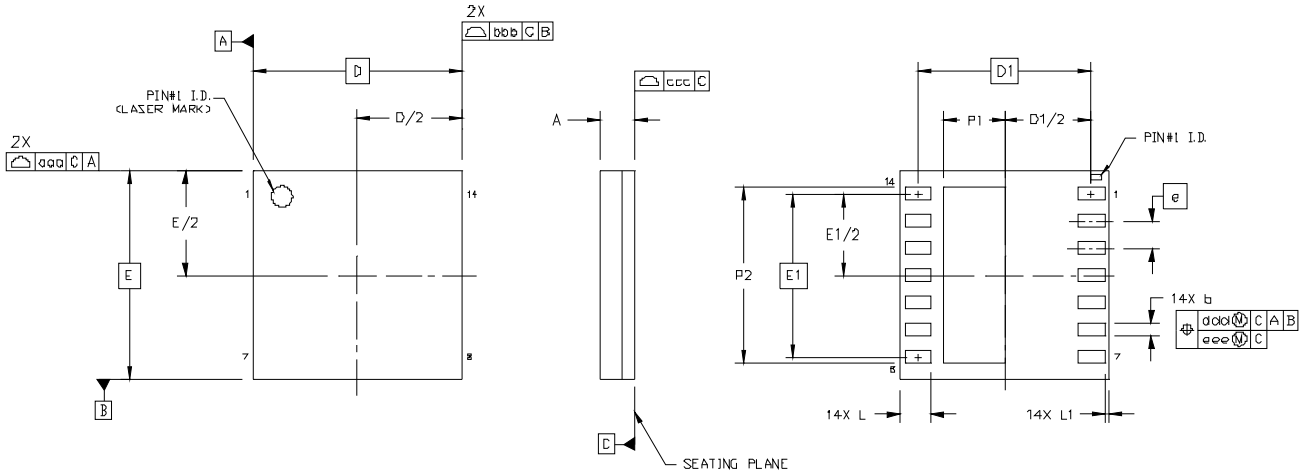


Figure 52. Si823x LGA Outline with Thermal Pad

Table 25. Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.74	0.84	0.94
b	0.25	0.30	0.35
D	5.00 BSC		
D1	4.15 BSC		
e	0.65 BSC		
E	5.00 BSC		
E1	3.90 BSC		
L	0.70	0.75	0.80
L1	0.05	0.10	0.15
P1	1.40	1.45	1.50
P2	4.15	4.20	4.25
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.15
eee	—	—	0.08

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

17. Land Pattern: 14 LD LGA with Thermal Pad

Figure 53 illustrates the recommended land pattern details for the Si8236 in a 14-pin LGA with thermal pad. Table 26 lists the values for the dimensions shown in the illustration.

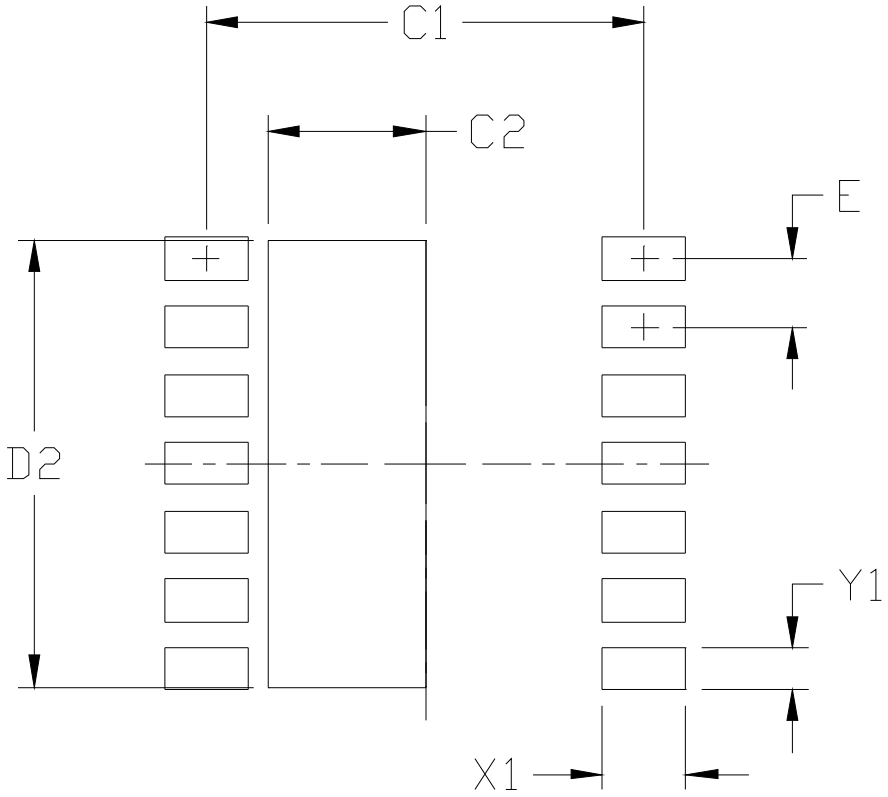


Figure 53. 14-Pin LGA with Thermal Pad Land Pattern

Table 26. 14-Pin LGA with Thermal Pad Land Pattern Dimensions

Dimension	(mm)
C1	4.20
C2	1.50
D2	4.25
E	0.65
X1	0.80
Y1	0.40

Notes:

General:

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design:

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design:

5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly:

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.11 to Revision 0.2

- Updated all specs to reflect latest silicon revision.
- Updated Table 1 on page 6 to include new UVLO options.
- Updated Table 2 on page 10 to reflect new maximum package isolation ratings
- Added Figures 34, 35, and 36.
- Updated Ordering Guide to reflect new package offerings.
- Added "5.6.3.Under Voltage Lockout (UVLO)" on page 25 to describe UVLO operation.

Revision 0.2 to Revision 0.3

- Moved Sections 2, 3, and 4 to after Section 5.
- Updated Tables 15, 16, and 17.
  - Removed Si8230, Si8231, and Si8232 from pinout and from title.
- Updated and added Ordering Guide footnotes.
- Updated UVLO specifications in Table 1 on page 6.
- Added PWD and Output Supply Active Current specifications in Table 1.
- Updated and added typical operating condition graphs in "3.Typical Operating Characteristics (0.5 Amp)" on page 16 and "4.Typical Operating Characteristics (4.0 Amp)" on page 18.

Contact Information

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:
https://www.silabs.com/support/pages/contacttechnicalsupport.aspx
and register to submit a technical support request.